

15 bit, 2nd Order Noise Shaped SAR @ 1MS/sec

Abstract:

Since the introduction of 90nm CMOS Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However the best performing ADCs from a power consumption point of view have 10bits of resolution and a signal bandwidth of <1MHz. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic which all benefit from faster CMOS technologies. This work aims to leverage this speed advantage through oversampling and noise shaping to achieve an ADC with greater precision.

Introduction

The most efficient ADCs are limited by thermal noise. The comparator adds thermal noise and the faster the SAR ADC the larger the comparator noise bandwidth and its total integrated noise. The first Panther ADC chip consisted of a 10 bit SAR core, a noise shaping loop filter use duty cycled open loop trans-conductance (GM) stages as integrators and a summing comparator. The performance of this ADC was limited by the wideband thermal noise of the GM stages and the fact that the integrators were designed for a fixed clock frequency.

Target Specifications:

Specification Name	Typical	Description
Sampling rate	75MS/s	rate at which input signal is sample 2ns S&H time
SAR clock rate (synchronous)	1.5GS/s	Synchronous timing uses an external clock
Resolution w/o shaping	10ENOB	resolution of SAR core 10bits + 2 redundant bits
Input signal bandwidth	1MHz	target signal frequency
Resolution with shaping	15ENOB	Target resolution for shaped ADC
SNDR @100kHz	90dB	Target resolution for signals at 1MHz
Supply voltage	0.9V	Use core supply if possible to reduce number of supply pins
Power	<5 mW	Power to create a competitive FoM

ADC Architecture and Model:

For the Panther2 ADC an error feedback topology had been implemented. The error feedback topology samples the residue at the end of one conversion and creates a gained version of the residue on a capacitor. This gained residue is capacitively subtracted from the next sampled value of the ADC input. A first order feedback filter has been used as this has the lowest circuit thermal noise. The residue sample and gain circuit uses a dynamic amplifier gain stage which allows the

loop filter thermal noise and power consumption to be reduced. Self-timing is added to the dynamic amplifiers to allow the loop filter to operate independently to the ADC rate.

Panther2v3 testing:

Panther2 revision 3 Silicon is in our lab. The core SAR behaves well but unfortunately the dynamic amplifier in the noise shaping loop is not working. To debug we have used the register controlled trim bits and analysed the current consumption of the Dynamic amplifier. We have also tested turning on and off the chopping mode and adding dc offsets to the first amplifier stage. On the parts we have tested none of these tests have allowed us to see the dynamic amplifier functioning the way we expect.

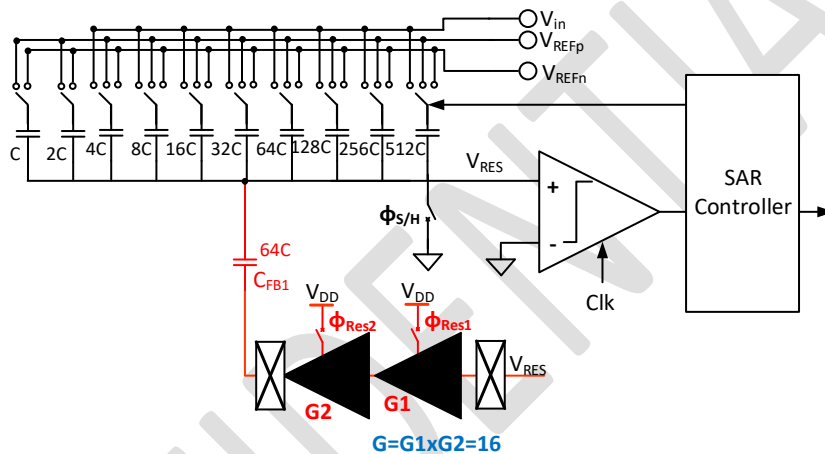


Figure 1: panther2v3 noise shaping path

Panther3 a new noise shaping topology:

A new MASH topology has been proposed. We believe this topology is less susceptible to thermal noise in the noise shaping loop than previously published topologies. The 2nd order shaping allows the core SAR resolution to be reduced to 6 bits. Fig.2 shows a diagram illustrating the operation of the topology. Residue voltages are stored at different times in the conversion cycle and then added back to the main capacitor bank. The digital code from the second conversion is differentiated to high pass filter its errors and noise. FFT plots of the ADC schematic and extracted simulation responses are shown in Fig. 3 and Fig. 4.

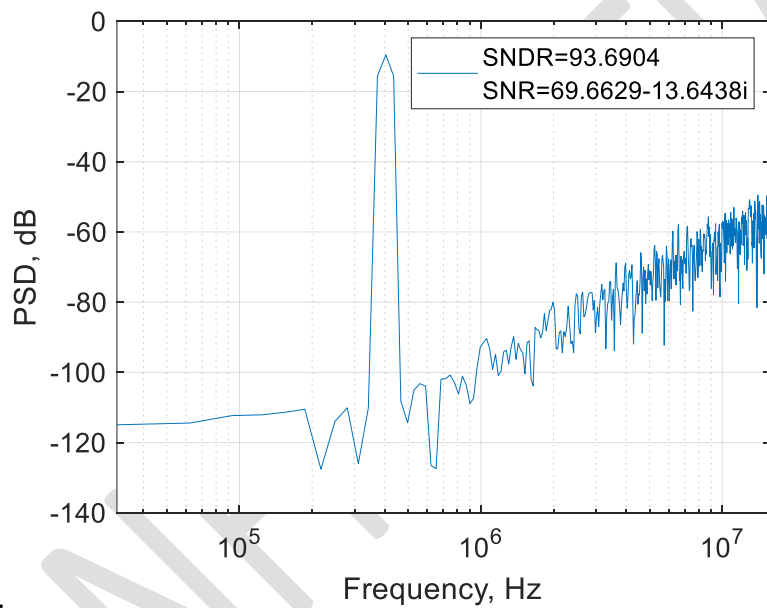
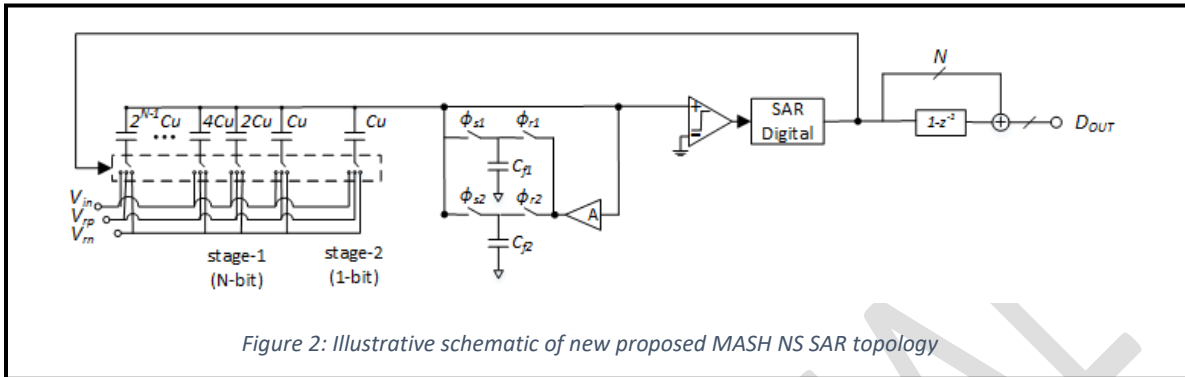


Figure 3: Schematic results for panther3

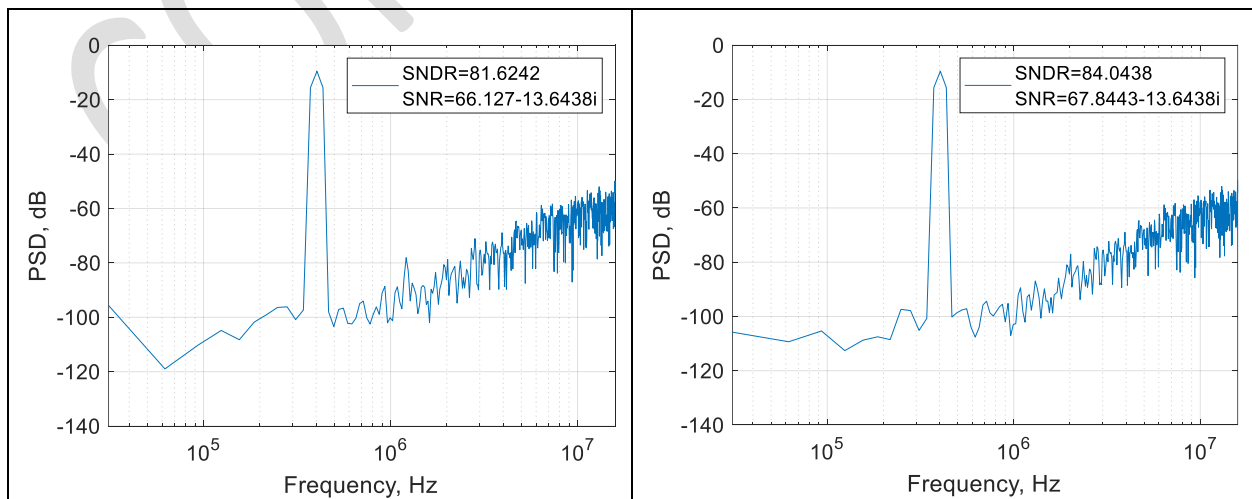


Figure 4: Simulated results of Analog core extracted (without calibration left and calibrated right)

Summary

Debug of Panther2v3 and preparation for testing of Panther 3 are ongoing.

Next Steps:

- Debug of Panther2v3 silicon parts.
- Prepare to test Panther 3

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