A multi-sensor Analogue Frontend using Time domain signal processing

Abstract:

We live in an Internet of Things (IoT) world where our environment and vital signs are monitored by hundreds of different sensors. Each iteration of the leading Smartphones incorporate more and more sensors. A traditional multi-sensor Analogue Frontend (AFE) consists of separate channels from each sensors. Each signal path is custom designed for a particular sensor and a mux connects the individual paths to a shared ADC. This implementation takes up a lot of chip area especially if the signals need large resistors and capacitors to filter out noise above 10kHz. Analogue to Digital converters have undergone a huge increase in performance in the 21st century. These improvements have meant that the power bottleneck in sensor systems is now the analogue interface not the ADC. The circuit techniques developed in this research project will be applicable to most sensor interfaces. The project will also leverage Tyndall Sensor Technology and know-how to enable new applications in the areas such as environmental monitoring. This work is applicable to the MCCI themes of Smart Agriculture, Connected Health and Industrial.

Introduction

This research project is primarily a circuits research project to design a robust adaptable sensor interface that can support Resistive, Capacitive, Voltage and Current mode sensors. A further goal will be to produce circuits that are lower in power and smaller in size than existing solutions.

Time based signal processing uses circuit blocks such as Time to Digital Converters (TDCs), VCOs, comparators and digital logic to convert sensor signal to digital. These circuits all benefit from process scaling so the performance and power consumption will improve at advanced CMOS processes unlike conventional analog signal processing. Fig. a, on the right, shows a conventional multi-sensor AFE. The ADC is shared but each sensor path is separate. Fig. c shows a resistance to time conversion circuit with a TDC to measure it. While different sensors have different voltage and frequency ranges a goal of the project will be to share circuitry between different resistive, capacitive, voltage and current paths to produce a low area solution. Dynamic circuits and duty cycling will be employed to minimise the interface power consumption.

ADCs are only as accurate as their voltage references. Time to digital converters are only as accurate as their time references. Part of this project work will investigate low area, low power time reference circuits which can be used to calibrate the TDC circuits so absolute accuracy can be achieved by the sensor interface.

Current work:

We are investigating methods to convert voltage and resistance to timing pulses. We are looking at the conversion equation for the measured signal and the various non-idealities, noise, flicker noise and mismatch that are added in the conversion. Fig. 2 shows a custom circuit for converting voltage to time in a feedback loop to convert a Delta-Sigma converter [1].

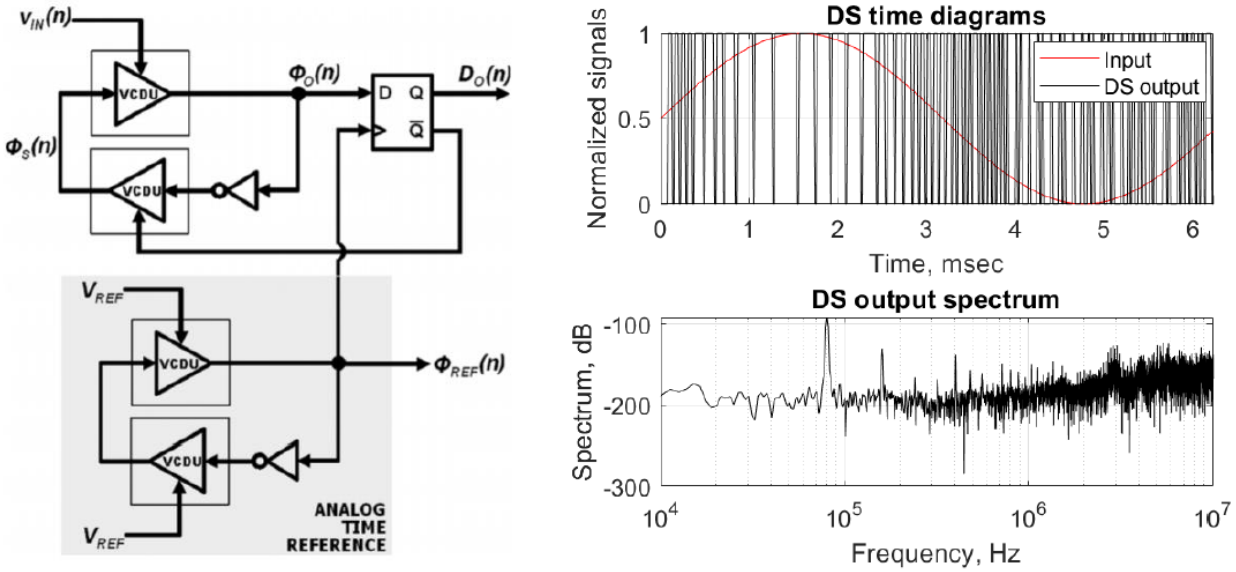

Figure 2: Delta-Sigma AtoD conversion via Time-mode signal processing [1]

Ramp based	VCO based	VCDU based	Sigma delta	Schmitt trigger based
- Linear - Wide DR	- Small chip area - Small power consumption	- Small chip area - Small power consumption	- Small chip area - Small power consumption - Noise shaping	- **Under review**
- Comparator offset mismatch	- Nonlinear TF - PVT sensitive	- Nonlinear TF - Low DR	- Hard to expand to high order	
Calibration	Polynomial correction [4]	Control through body node [6]	Extra time to voltage converters	

Figure 3: Summary of different voltage to time conversion techniques

Time to Digital Converters (TDCs)

We are investigating TDCs to identify the most suitable architectures. The sensor signal needs to be converted into a pulse and then digitized by the TDC, we need to investigate if an oversampled ADC will require many extra pulses to be generated. Fig. 2 shows a Delta Sigma TDC that could be used in an oversampled ADC.

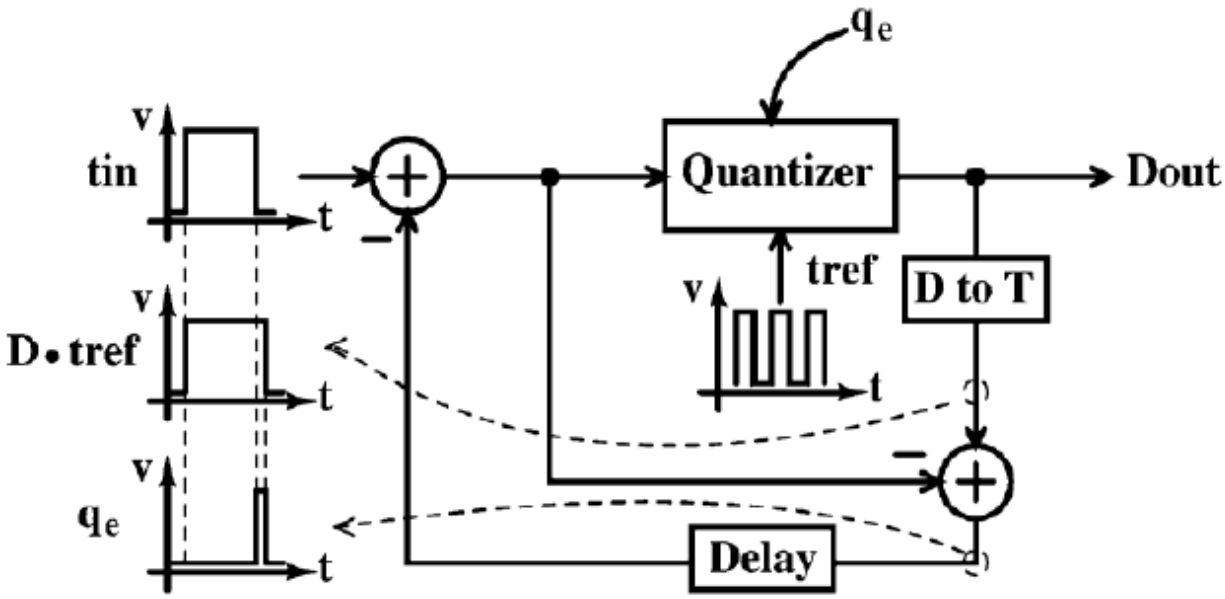

Figure 2: Delta Sigma TDC [2]

Next Steps:

- Continue investigating the key circuits
- Work on the application so we have a real specification to design for.

References

[1] Christopher S. Taillefer, Student Member, IEEE, and Gordon W. Roberts, Fellow, IEEE, "Delta–Sigma A/D Conversion Via Time-Mode Signal Processing," in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 56, NO. 9, SEPTEMBER 2009, doi

[2] Ying Cao, WouterDe Cock, MichielSteyaert, Paul Leroux, "1-1-1 MASH ΔΣ Time-to-Digital Converters With 6 psResolution and Third-Order Noise-Shaping," in IEEE Journal of Solid-State Circuits (Volume: 47, Issue: 9, Sept. 2012)