AI-Defined Power DAC/Transmitter

Abstract:

Recently, aiming to support higher data rate, there has been a significant interest in 5G wireless communication by exploiting larger bandwidth available at mm-wave frequencies. Analog power amplifiers (PAs) have been dominant at mm-wave frequencies. Recently, an outphasing transmitter (TX) and a Doherty PA were introduced in the Ka-band, obtaining high efficiency (>30%) and high output power (>20dBm). Outphasing and Doherty have been dependable techniques to improve the back-off efficiency but require complex passive networks. Inverse class-D architectures lead to high voltage stress on the output-stage devices. Additionally, at mm-wave, distributed effects contribute significantly to load-impedance variation, resulting in reduced output power. Voltage-mode switched-capacitor RFDACs (SCPAs) have proven nearly optimal for wireless TXs in CMOS because they occupy small chip area, are energy efficient and benefit from scaling. The SCPA is a segmented class-D amplifier, where the switches and capacitors are segmented in parallel paths that are digitally enabled/disabled to provide linear amplitude control. In this project, we will operate an SCPA in the mm-wave regime, which is enabled by the proposed edge combining technique, and in-slice LO generation with a careful design of distributed effects in the capacitor array. Further improving the performance of SCPA, we also aim to improve performance in terms of the EVM and ACLR performance. Consideration of smart calibration to improve performance of the proposed SCPA will be investigated to achieve state-of-the-art performance Ka band digital transmitter suitable for 5G communication.

Target Specification:

In this project, we aim to improve efficiency of the mm-wave digital PA with reduced area. It should support high order modulation scheme with large bandwidth (>200MHz@28GHz). The target output power is in the range of 19dBm – 24dBm while avoiding any voltage stresses on the transistor core devices to ensure reliability and improve its lifetime. Due to the proposed edge combining technique, a smart-calibration scheme will be investigated to reduce any spurious arising from phase mismatches, and thus it can further improve EMV and ACLR performance. Based on the comparison with digital I/Q, polar transmitter techniques, digital outphasing technique will be extensively investigated due to its advantages for higher efficiency (exploiting constant envelope) while maintaining small area.

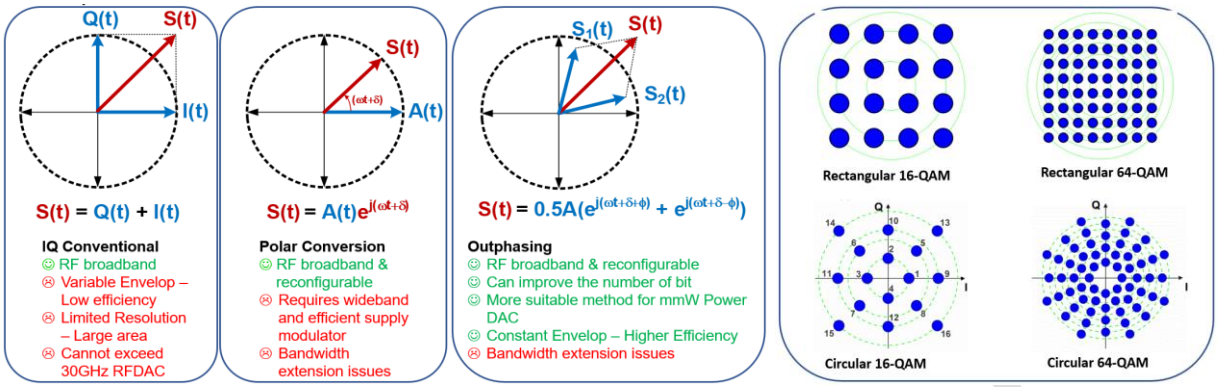

Fig .1. (a) Comparison among I/Q, Polar, outphasing techniques; (b) possible modulation schemes for outphasing technique

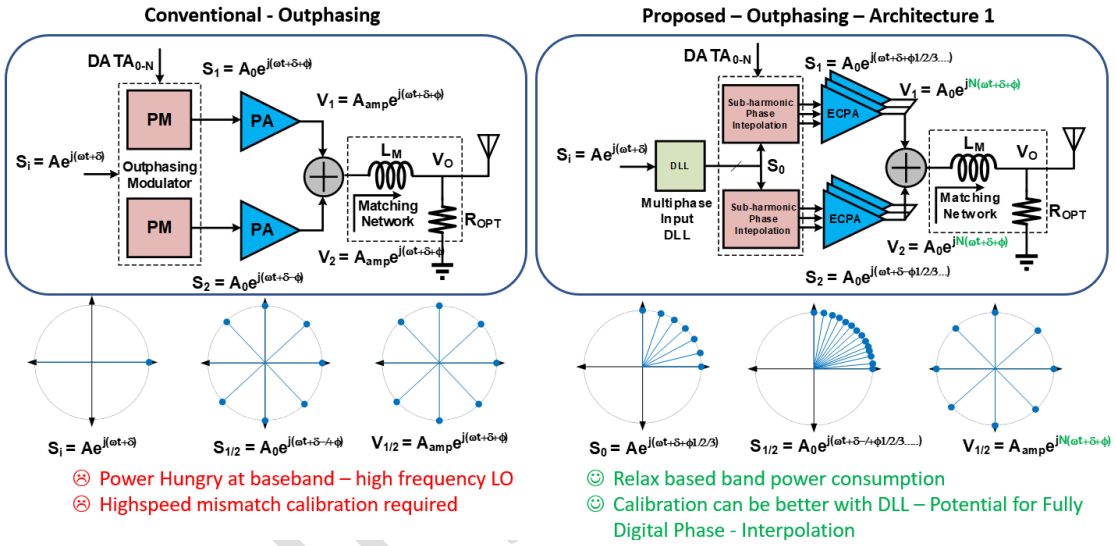

Fig .2. The comparison of the conventional outphasing architecture and the proposed outphasing SCPA architecture with edge/frequency combining technique.

Proposed Outphasing RF-DAC architecture:

As briefly mentioned in the previous section, this work aims to improve the efficiency of the design through Switch-Capacitor RFDAC with outphasing technique and boosting the frequency of operation to 28GHz by means of the proposed edge/frequency combining technique. Instead of relying on power hungry LO generation, in this pork, we propose to use multiphase delay-locked loop (DLL) which helps relaxing power consumption of the baseband circuitry. Moreover, accurate control of each phase from DLL can potentially be utilized for further calibration. To accommodate complex modulation scheme with the high frequency, the Circular QAM can provide better BER vs. SNR when compared to the rectangular QAM. This will be sufficient for higher frequency application and also fit well with the proposed multi-phase outphasing architecture where the I/Q phases can be combined at different space-state for generating desired symbol.

The propose architecture contains the high-speed multiphase clock generation which generates multi-phase clock at its sub-harmonic frequency. This is achieved by the DLL as shown in Fig. 2 (b). Moreover,

the phase multiplexing will be integrated into the interpolated block to achieve desired the modulation scheme. The modulated sub-harmonic phases will be fed into the edge/frequency combining SCPA for frequency upconversion to mmW frequency. It is then fed to the transimpedance matching network to feed to the antennas. The calibration path senses the output power from the PA by means of the sensing path which will include a down-conversion circuit for calibration processing to improve the accuracy and reduce potential spurious arising from the phase mismatches in the proposed architecture.

The breakdown of required building blocks in the proposed architecture is summarized below:

- Edge combining power amplifier design
- Power combiner with low loss and feedback sensing path
- Delay-locked loop (DLL) and oscillator coupling network implementation
- Sub-harmonic interpolation and phase selection
- Smart-Calibration (can be AI or neural network) feed-back and scheme

Based on our latest simulation result with parasitic extraction (see Fig. 3), the proposed 'edge/frequency-combining' SCPA obtained very good performance with the drain efficiency nearly the same at low frequency (60%). The optimization of the power combiner is on-going to achieve better efficiency in order to maintain the output efficiency at higher than 42% (see Fig. 4).

Here is the summary of upcoming plan for this project:

- Continue optimizing the efficiency and the architecture of the edge combining PA
- Detailed design and optimization of other building blocks: DLL, phase interpolation, etc.
- Smart calibration scheme and implementation.
- Tapeout is expected in 11/2021.

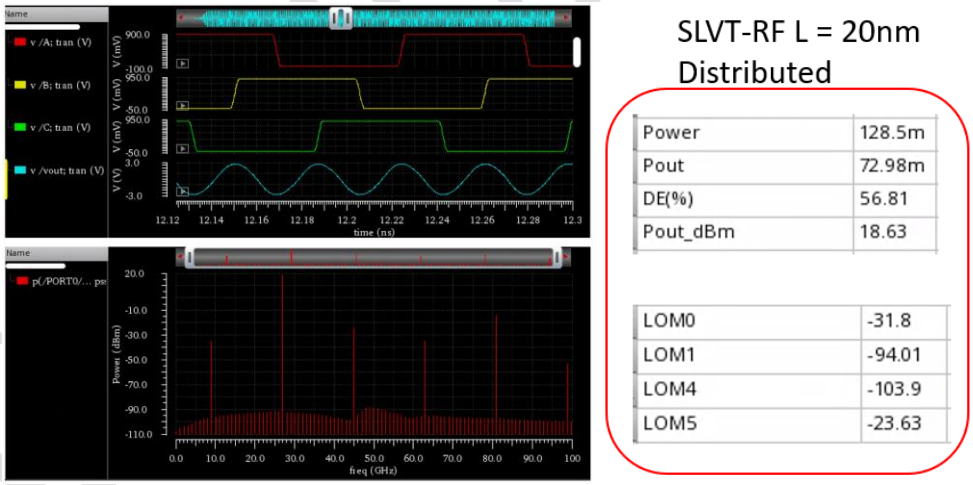

Fig .3. Simulation result of the SCPA with edge/frequency combining technique which shows output power of 19dBm and the drain efficiency obtain 56.81% at 28GHz.

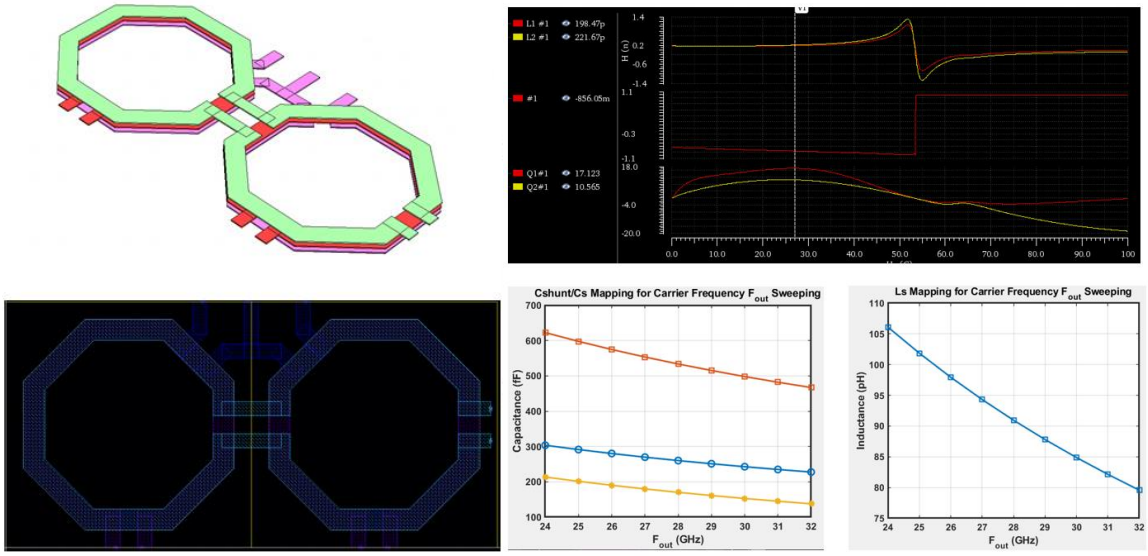

Fig .4. 3D EM modelling and layout of the proposed power combiner and matching network with R_{opt} = 4 Ohm, Q_{load} = 4 at 28GHz for efficiency improvement