

# Magnetic Field Sensor and Analog Front End for Medical Position Tracking.

## Abstract:

Electromagnetic tracking (EMT) is a key enabling technology for image-guided medical interventions. Commercial EMT systems enable catheter, neurosurgery and flexible endoscopy tool tracking. However there are shortcomings with current solutions viz. large coil-based sensors, susceptibility to noise and interference, large system latency etc. This project will implement a SoC solution to address many of these shortcomings. Mixed-signal ASIC/SoC benefits include: smaller devices, better accuracy, wireless integration, faster systems and reduced noise.

## Introduction:

We are proposing to develop a new SoC Receiver architecture with focus on the following novelties:

- First CMOS-based EMT implementation platform suitable for endoscope integration
- First integrated inductive sensor suitable for <1mm tracking applications
- First integrated high-resolution ADC for low-latency read-out of sensor voltage
- 4X improvement in accuracy and noise suppression compared to discrete coil
- 10x improvement in system latency compared to current commercial and clinical systems through minimal transmission delays, single-die implementation enabling near real-time tracking (not possible with current 30-40ms latency in commercial OEM platforms such as NDI Aurora). Very important for robotic surgery integration
- Significantly reduced EMI susceptibility through integrated inductive loops and on-chip calibration for noise compensation.

The Receiver will consist of an integrated magnetic sensor coil, analogue signal filtering & conditioning, 16-bit ADC for digital signal conditioning, 1 mm<sup>2</sup> package SoC solution for immediate integration and testing with Anser. We aim to use standard 28nm TSMC General Purpose processes and integrated Ferric for CMOS BEOL integrated magnetic material.

## Target Specs:

- Magnetic field sensitivity ~ 1 mV/T (voltage mode sensing)
- Sensor bandwidth < 100 kHz
- AFE: min detectable signal 1uV
- IC area: Height < 0.5mm, Width <5mm

**System Architecture:**

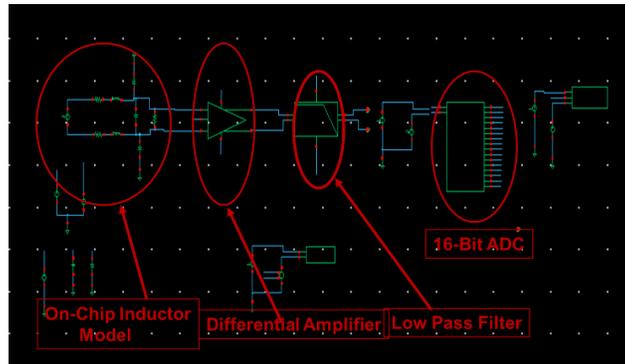


Figure 1. ANSER Receiver Architecture

**Results to Date:**

*On Chip Inductor Modelling:*

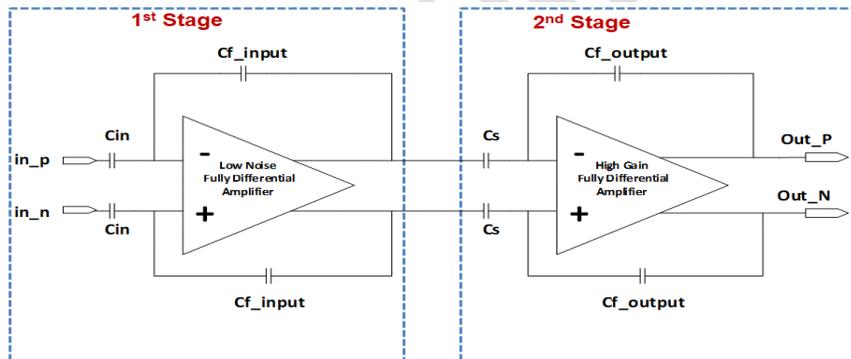


Figure 2. Our 2-stage amplifier configuration is designed to minimize noise using fully differential capacitive feedback on both stages.

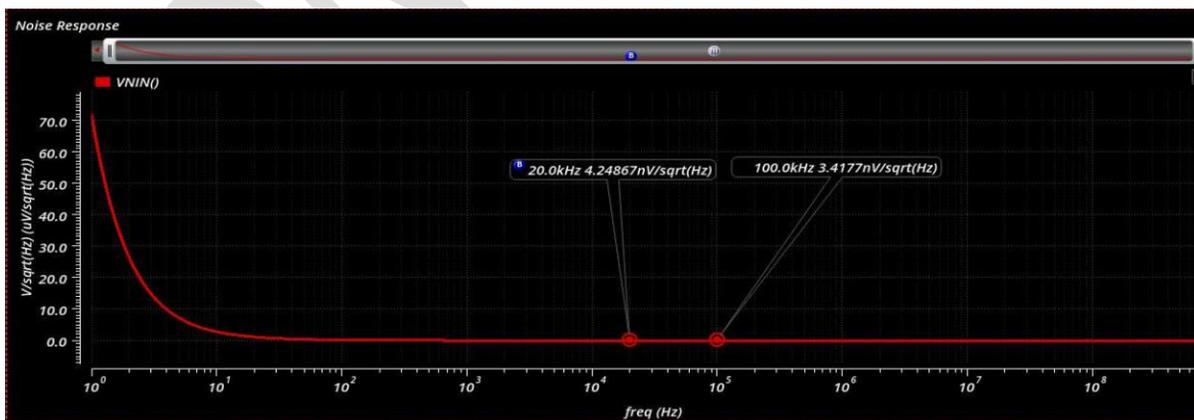


Figure3. Noise Results for FE Low Noise Amplifier

Input Frequency(KHz)	Spec Noise Density( $nV/\sqrt{Hz}$ )	Measured Noise Density( $nV/\sqrt{Hz}$ )	Spec Flicker Noise Corner	Measured Flicker Noise Corner
20	2	4.2	<10KHz	9KHz
100		3.41		

Table1. Noise Results for FE Low Noise Amplifier

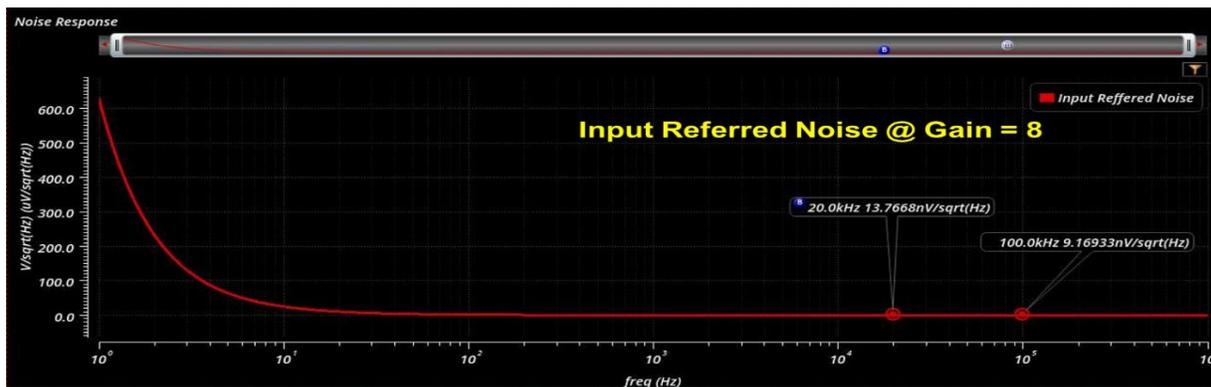


Figure4. Noise Results for 2<sup>nd</sup> Stage Programmable Amplifier

Input Frequency(KHz)	Spec Noise Density( $nV/\sqrt{Hz}$ )	Measured Noise Density( $nV/\sqrt{Hz}$ )	Spec Flicker Noise Corner	Measured Flicker Noise Corner
20	10	13.7	<10KHz	13KHz
100		9.1		

Table2. Noise Results for 2nd Stage Programmable Amplifier

Observation: The flicker noise from Differential pairs is main contributor towards total input referred noise of FE Low noise amplifier.

### Amplifier Specifications:

Spec Name	Min	Typ	Max	Simulated Results
Input Referred Noise		$2nV/\sqrt{Hz}$		$4.2nV/\sqrt{Hz}$
Power			6mW	
Offset				
Flicker Noise Corner		<10KHz		9KHz
Area		$360 \times 320 \mu m^2$		
Input Voltage(P-P)	1uV		1mV	
Output Voltage Swing (P-P)	20uV		20mV	
Gain (Vo/Vi)		20		
PSSR		-50dB		-42dB
CMMR		-50dB		-52dB
Power Supply		1.2		
Signal Frequency		20KHz	100KHz	
Input Common Mode		0V		
Output Common Mode		600mV		
PM		60°		75°

Table 3. FE Amplifier specifications on full system simulations.

Spec Name	Min	Typ	Max	Simulated Result
Input Referred Noise@20KHz		10n V/ $\sqrt{Hz}$		7.08n V/ $\sqrt{Hz}$
Power		4mW		4.9mW
Output Offset		50mV		
Flicker Noise Corner		10KHz		13KHz
Area				
Input Voltage(P-P)	3 $\mu$ V		20mV	
Output Voltage Swing (P-P)	120uV		0.8V	
Gain (Vo/Vi)	8		40	
PSSR@100KHz		-50dB		-191dB
CMMR@100KHz		-50dB		-210dB
Power Supply		1.2		
Signal Frequency		20KHz	100KHz	
Input Common Mode		150m		
Output Common Mode		600m		580m
Programmable Gain Fully differential Amplifier PM		50 $^{\circ}$		86 $^{\circ}$

Table 4. 2<sup>nd</sup> Stage Programmable Amplifier specifications on full system simulations.

### Transient Noise Analysis Results:

- Input Signal : 1mV(P-P) @100khz
- FE Amplifier Gain = 20
- 2<sup>nd</sup> Stage Amplifier Gain = 8
- Switch(Duty Cycle Resistor) frequency : 250KHz
- Auto Zero Switch Frequency : 3KHz
- Sampling Frequency : 13MHz
- No of Samples : 131072
- BW = 100 Hz

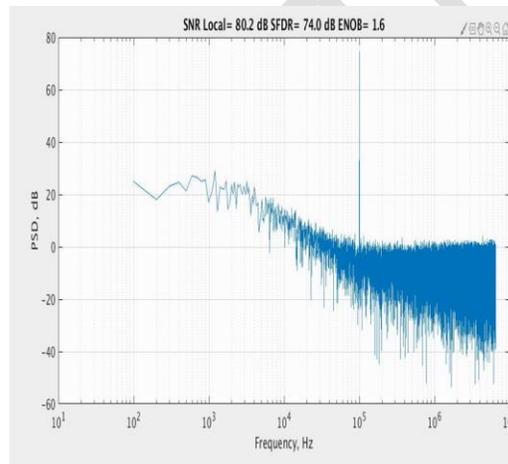


Figure 5. Transient noise simulation result on full system simulations.

### We have taped out 4 Chips variants in June 2020.

Chip	Inductor	FE Amplifier	2nd Stage Amplifier	Comment
A	M8(117 Turns)	Gain Boost	Gain Boost	
B	M9(38 Turns)	No GB	NO GB	
C	M9(38 Turns)	Chopping	Gain Boost	
D	M8(40 N) + M9(37 N) + M10 (22 N)	Gain Boost	Gain Boost	Debug Version Pin Out for Inductor and amplifier

PCB design has been completed and sent for fabrication.

### Next Steps:

- Series 1 testing (Oct 2020)
- Paper Writing (Jan 202)