Magnetic Field Sensor and Analog Front End for Medical Position Tracking.

Abstract:

Electromagnetic tracking (EMT) is a key enabling technology for image-guided medical interventions. Commercial EMT systems enable catheter, neurosurgery and flexible endoscopy tool tracking. However there are shortcomings with current solutions viz. large coil-based sensors, susceptibility to noise and interference, large system latency etc. This project will implement a SoC solution to address many of these shortcomings. Mixed-signal ASIC/SoC benefits include: smaller devices, better accuracy, wireless integration, faster systems and reduced noise.

Introduction:

We are proposing to develop a new SoC Receiver architecture with focus on the following novelties:

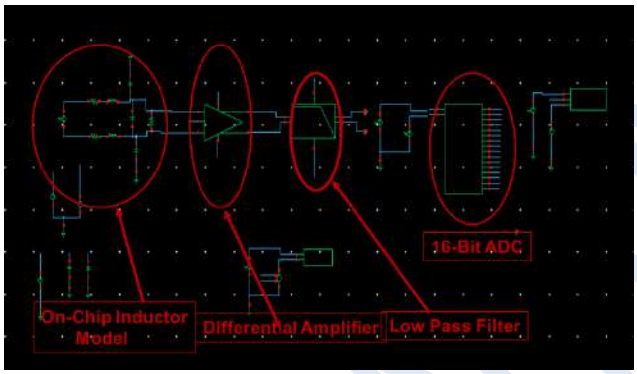
- First CMOS-based EMT implementation platform suitable for endoscope integration
- First integrated inductive sensor suitable for <1mm tracking applications
- First integrated high-resolution ADC for low-latency read-out of sensor voltage
- 4X improvement in accuracy and noise suppression compared to discrete coil
- 10x improvement in system latency compared to current commercial and clinical systems through minimal transmission delays, single-die implementation enabling near real-time tracking (not possible with current 30-40ms latency in commercial OEM platforms such as NDI Aurora). Very important for robotic surgery integration
- Significantly reduced EMI susceptibility through integrated inductive loops and on-chip calibration for noise compensation.

The Receiver will consist of an integrated magnetic sensor coil, analogue signal filtering & conditioning, 16-bit ADC for digital signal conditioning, 1 mm2 package SoC solution for immediate integration and testing with Anser. We aim to use standard 28nm TSMC General Purpose processes and integrated Ferric for CMOS BEOL integrated magnetic material.

Target Specs:

- Magnetic field sensitivity ~ 1 mV/T (voltage mode sensing)
- Sensor bandwidth < 100 kHz
- AFE: min detectable signal 1uV
- IC area: Height < 0.5mm, Width <5mm

System Architecture:



Results to Date:

On Chip Inductor Modelling:

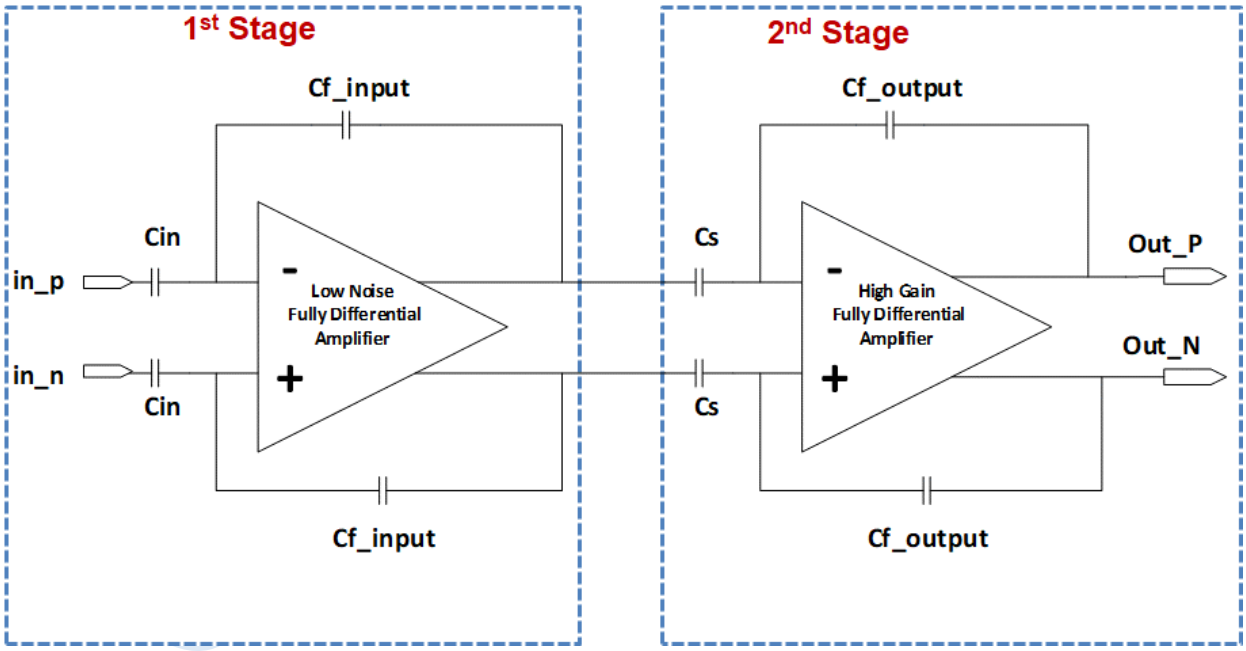


Figure 1. Our 2-stage amplifier configuration is designed to minimize noise using fully differential capacitive feedback on both stages.

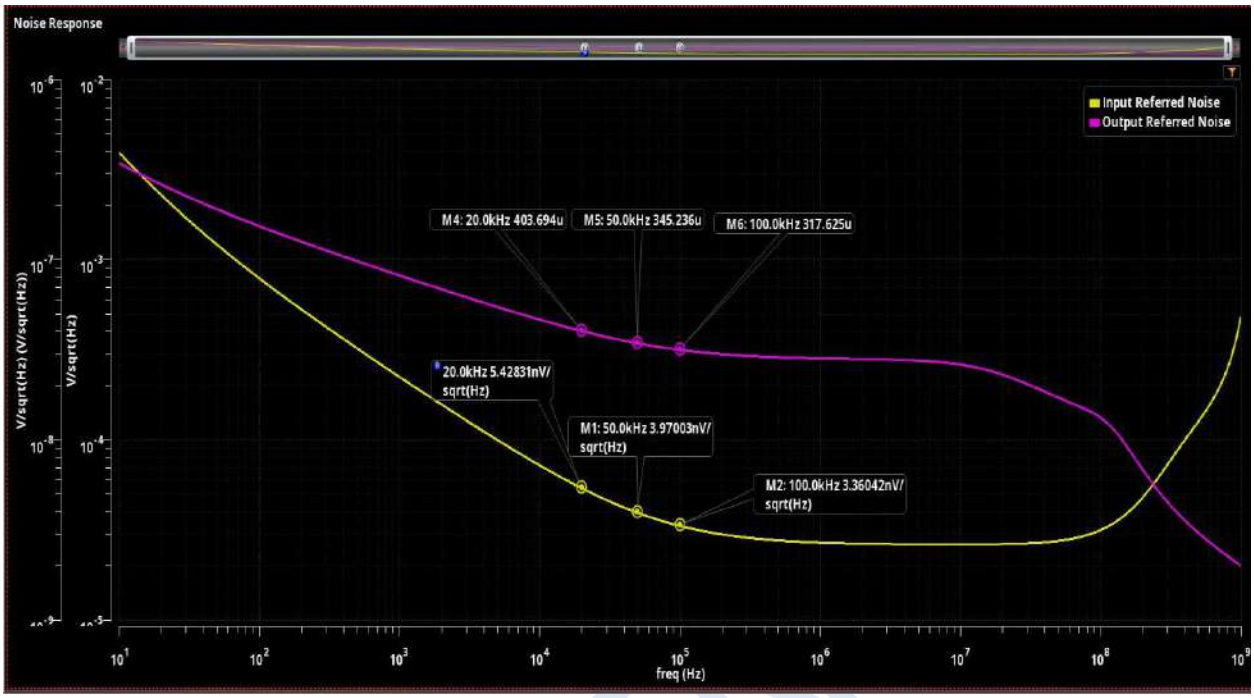


Figure2. Noise Results for FE Low Noise Amplifier.

Input Frequency(KHz)	Spec Noise Density(nV/$\sqrt{Hz}$)	Measured Noise Density(nV/$\sqrt{Hz}$)	Spec Flicker Noise Corner	Measured Flicker Noise Corner
20	2	5.42	<10KHz	40.7KHz
50		3.97		
100		3.36		

Figure3. Noise Results for FE Low Noise Amplifier.

Observation: The flicker noise from Differential pairs is main contributor towards total input referred noise of FE Low noise amplifier.

Amplifier Specifications:

Spec Name	Min	Typ	Max
Input Referred Noise		2n V/$\sqrt{Hz}$	
Power			5mW
Offset			
Flicker Noise Corner		3.5KHZ	
Area		352x396µm^2	
Input Voltage(P-P)	150nV		1mV
Output Voltage Swing (P-P)	3.0uV		20mV
Gain (Vo/Vi)		20	
PSSR			
CMMR			
Power Supply		1.2	
Signal Frequency		20KHz	100KHz
Input Common Mode		0V	
Output Common Mode		600mV	
PM		60^0	

Figure 2. Updated amplifier specifications based on full system simulations.

Next Steps:

- Design Review 3 (April 2020)
- Series 1 tape-out on 65nm (May 2020)
- Test-board design and build (June 2020)
- IP filing (July 2020)
- Series 2 design planning (Aug 2020)
- Series 1 testing (Sept 2020)