Magnetic Field Sensor and Analog Front End for Medical position tracking.

Abstract:

Electromagnetic tracking (EMT) is a key enabling technology for image-guided medical interventions. Commercial EMT systems enable catheter, neurosurgery and flexible endoscopy tool tracking. However there are shortcomings with current solutions viz. large coil-based sensors, susceptibility to noise and interference, large system latency etc. This project will implement a SoC solution to address many of these shortcomings. Mixed-signal ASIC/SoC benefits include: smaller devices, better accuracy, wireless integration, faster systems and reduced noise.

Introduction:

We are proposing to develop a new SoC Receiver architecture with focus on the following novelties:

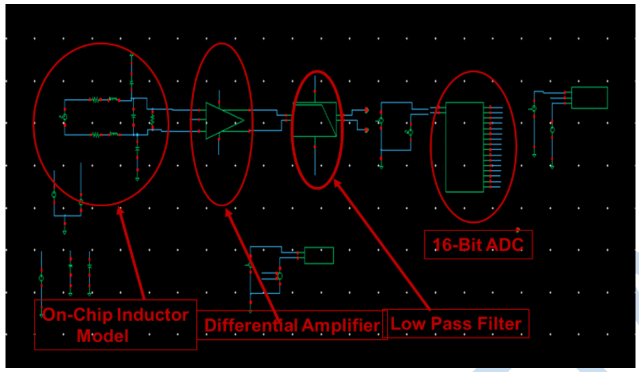
- First CMOS-based EMT implementation platform suitable for endoscope integration
- First integrated inductive sensor suitable for <1mm tracking applications
- First integrated high-resolution ADC for low-latency read-out of sensor voltage
- 4X improvement in accuracy and noise suppression compared to discrete coil
- 10x improvement in system latency compared to current commercial and clinical systems through minimal transmission delays, single-die implementation enabling near real-time tracking (not possible with current 30-40ms latency in commercial OEM platforms such as NDI Aurora). Very important for robotic surgery integration
- Significantly reduced EMI susceptibility through integrated inductive loops and on-chip calibration for noise compensation.

The Receiver will consist of an integrated magnetic sensor coil, analogue signal filtering & conditioning, 16-bit ADC for digital signal conditioning, 1 mm2 package SoC solution for immediate integration and testing with Anser. We aim to use standard 28nm TSMC General Purpose processes and integrated Ferric for CMOS BEOL integrated magnetic material.

Target Specs:

- Magnetic field sensitivity ~ 1 mV/T (voltage mode sensing)
- Sensor bandwidth < 100 kHz
- AFE: min detectable signal 1uV
- IC area: Height < 0.5mm, Width <5mm

System Architecture:



Results to Date:

On Chip Inductor Modelling:

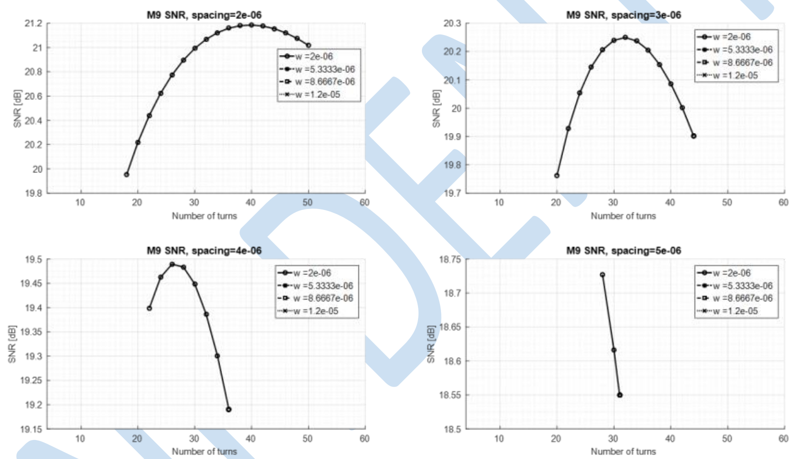


Figure 1. Optimised simulated SNR has identified optimal line and spacing for single-layer on-chip inductor. We are currently working to extend this analysis to multi-layer coils which will be used for magnetic field sensing on-chip.

Amplifier Simulation:

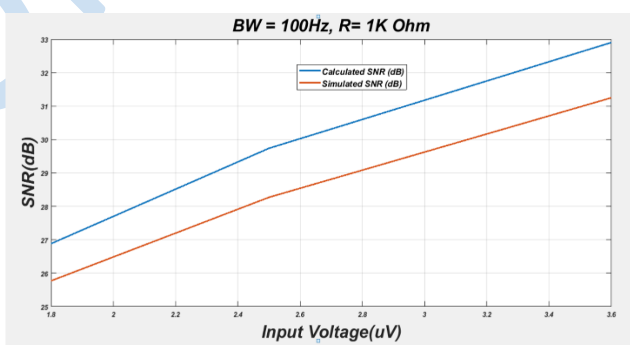


Figure 2. Updated amplifier assuming differential ended mode for calculated (analytical) and simulated input with 100 Hz sampling bandwidth and 1k Ohm coil input impedance.

Next Steps:

- Coil geometry layout and simulation for multi-layer geometry (Oct 2019)
- Amplifier SNR analysis and design completion (due Nov 2019)
- Series 1 tape-out (Jan 2020)