

Charge-Sharing Locking Fractional- N Frequency Synthesis

Yizhe Hu and Robert Bogdan Staszewski

Abstract:

Ultra-low jitter (sub-100fs/50fs) frequency synthesis is highly desirable for 5G/6G RF and mm-Wave (mmW) communications to support the complex modulation schemes (e.g., 1024QAM). The idea of charge-sharing locking is that the capacitor of the LC tank itself will be periodically charge-shared with another capacitor charged by a DAC to a voltage that is expected from a waveform at that particular time point, resulting in an instantaneous phase correction. The resulting voltage change will be detected and used to correct the DCO frequency. This results in a great simplification of circuitry and consumed power while delivering sub-100fs integrated jitter.

1. Proposed CSL architecture:

Figure 1 shows the basic concept of charge-sharing locking (CSL). At the heart lies the LC-tank oscillator generating a (near) sinusoidal waveform of frequency. During the high-level of reference clock ref , the digital logic (DIG) driving the DAC presets V_{share} on the sharing capacitor C_{share} (via switch S_1) to the expected oscillator waveform voltage at the significant reference instances (defined as ref 's falling edges. Afterwards, a narrow pulse shortly connects C_{share} to C_{osc} (i.e., S_1 OFF, S_2 ON) for the actual CSL operation. After the charge-sharing operation with the oscillator is completed, the charge residue leftover in the C_{share} will contain information of the frequency deviation. This voltage is digitized by a SAR-ADC upon asserting clk_q_trans . The ADC output is passed through the DZ, accumulator, and attenuation factor KI (affecting the convergence speed) to generate the oscillator tuning word (OTW).

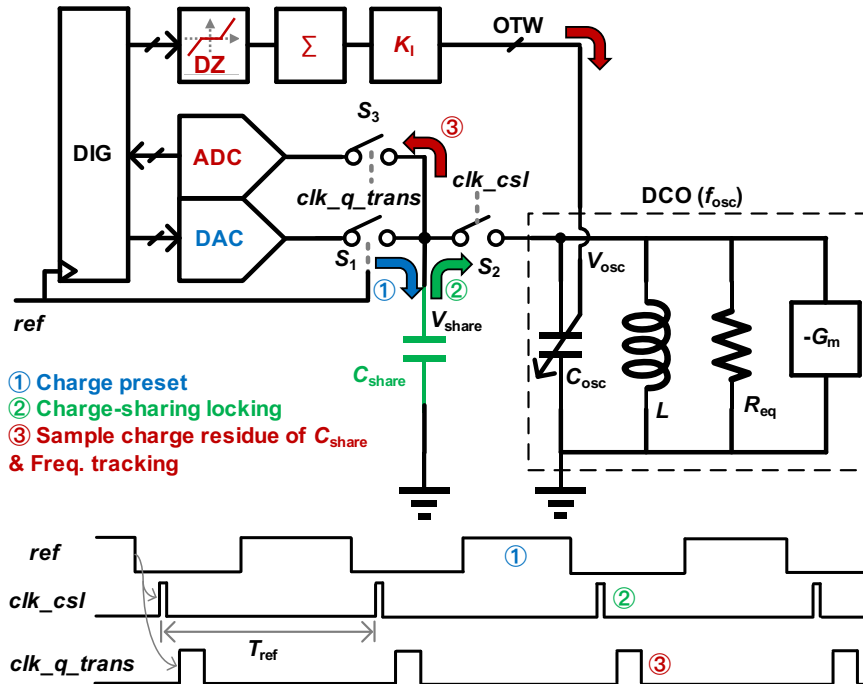


Fig .1. Basic architecture of charge-sharing locking.

2. Proposed Digital-to-Time Converter

To support fractional- N operation in CSL, a high-performance digital-to-time converter based on RC -delay is introduced. Several techniques are employed to mitigate the nonlinearity of DTC, including linearized R and C , dummy cap-bank for stabilizing the supply ringing, etc. The post simulated performance of DTC is shown in Fig. 2, achieving 9-bits, LSB: ~ 500 fs, INL: < 0.3 LSB, power < 0.5 mW.

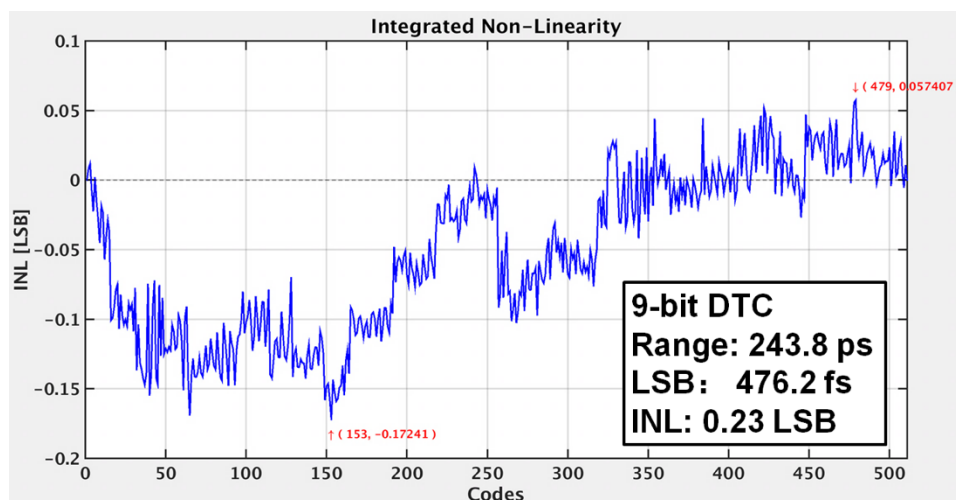


Fig .2. Post simulation of the proposed digital-to-time converter (DTC) supporting fractional- N CSL.

3. Simulation Results

Fig. 3 shows the post-simulated rms jitter and spur performance. It achieves sub-30 fs and sub-50 fs rms jitter for integer-N and fractional-N operation. Due to the high-linearity of the proposed DTC, the in-band spur is around -59 dBc. To the best of authors' knowledge, this is the best performance for fractional-N PLL, demonstrating the advantage of CSL.

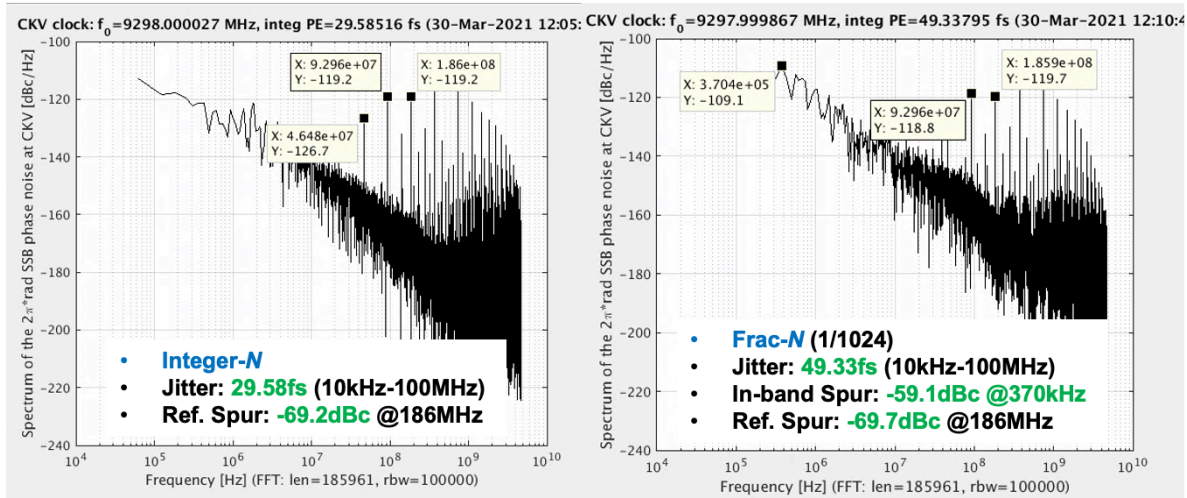


Fig. 3 Simulated rms jitter and spur performance for CSL: (a) Integer-N operation (b) Fractional-N operation (fractional number = 1/1024).

4. Future work:

- Final check schematic and layout, and plan to tape-out in April 2021 with TSMC LP 28nm
- Prepare PCBs and measurements