Panther

Abstract:

Since the introduction of 90nm CMOS Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However the best performing ADCs from a power consumption point of view have 10bits of resolution and a signal bandwidth of <1MHz. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic which all benefit from faster CMOS technologies. This work aims to leverage this speed advantage through oversampling and noise shaping to achieve an ADC with greater precision.

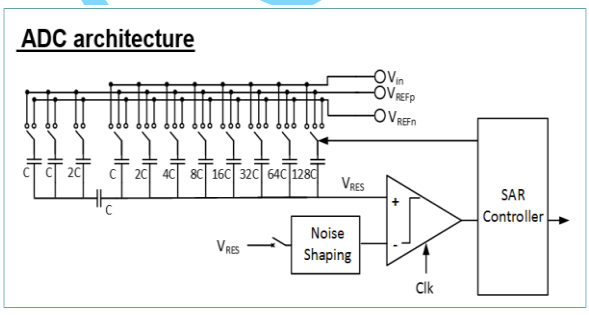
Introduction

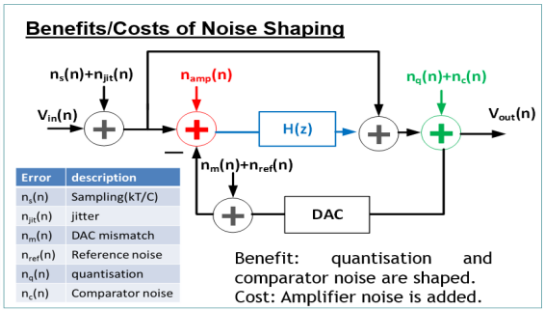
The most efficient ADCs are limited by thermal noise. The comparator adds thermal noise and the faster the SAR ADC the larger the comparator noise bandwidth and its total integrated noise. Our proposed noise shaped SAR ADC consists of a 10 bit SAR core, a noise shaping loop filter and a summing comparator. The SAR conversions take place followed by the residue sampling. We use duty cycled open loop trans-conductance (GM) stages as integrators. A feedforward loop filter topology is used.

Target Specifications:

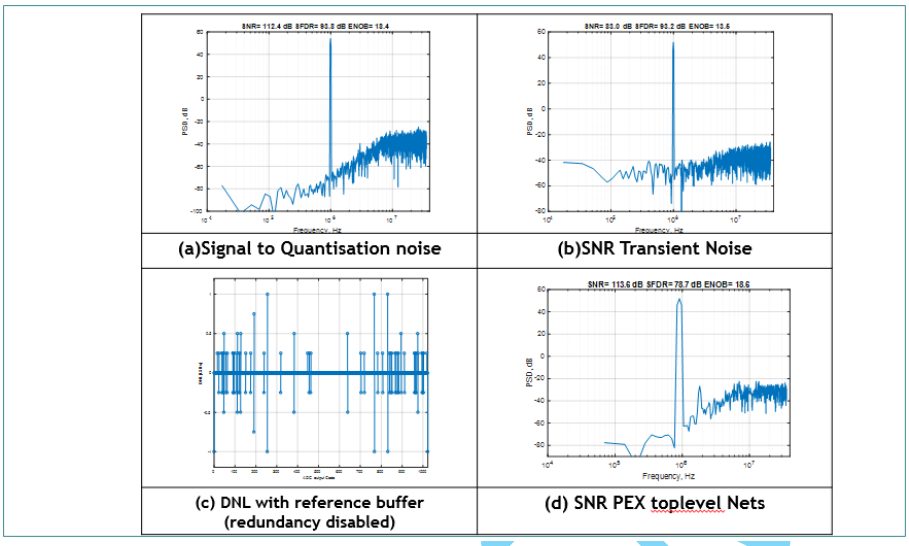
Specification Name	Typical	Description
Sampling rate	75MS/s	rate at which input signal is sample 2ns S&H time
SAR clock rate (synchronous)	1.5GS/s	Synchronous timing uses an external clock
Resolution w/o shaping	10ENOB	resolution of SAR core 10bits + 2 redundant bits
Input signal bandwidth	1MHz	target signal frequency
Resolution with shaping	15ENOB	Target resolution for shaped ADC
SNDR @100kHz	90dB	Target resolution for signals at 1MHz
Supply voltage	0.9V	Use core supply if possible to reduce number of supply pins
Power	<5 mW	Power to create a competitive FoM

ADC Architecture and Model:



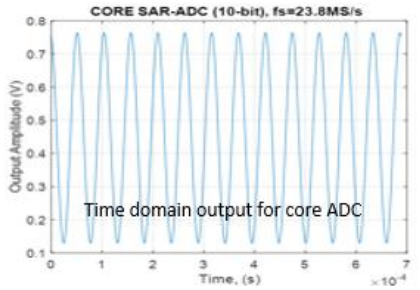


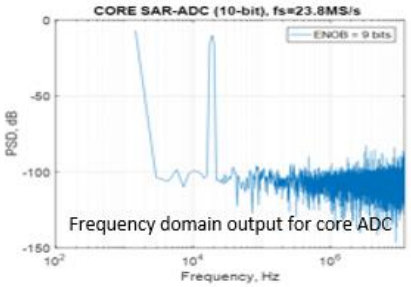
Simulation Results:

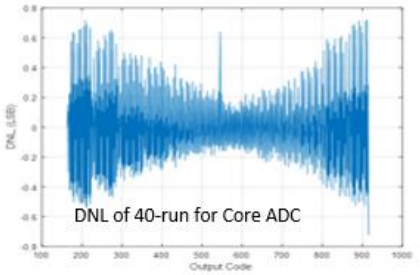


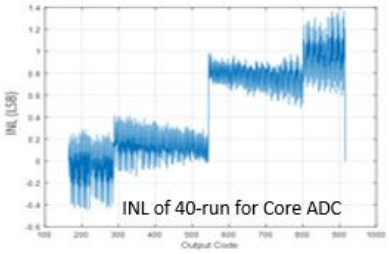
Tapeout Date: June 2018.

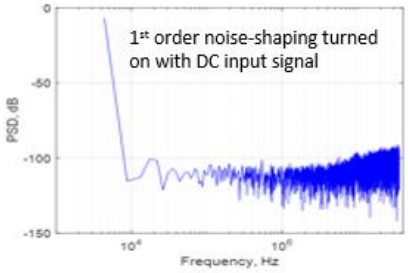
Measured Results:

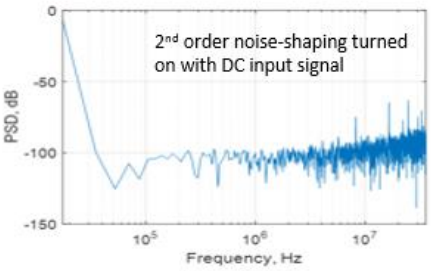












Summary

Silicon broadly matches simulations except for noise shaping (under debug). SAR Core DNL < 0.5LSB, INL < 1LSB. The spec was DNL<0.3LSB and INL<0.5 LSB. In band noise floor in SAR is -83dB.

We have a good SAR core performance that we are making incremental improvements to and we have identified the test problems that we have to solve. We are debugging the performance issue with 2nd order noise shaping. For next tapeout, we are redesigning the noise shaping to have lower noise and to make it work at all clock frequencies.

Next Steps:

Panther1 noise shaping only works with a 1.5GHz clock and is limited by circuit noise.

- We are redesigning the noise shaping to have lower noise and to make it work at all clock frequencies < 1.5GHz and has lower circuit noise.
- Based on measurements improve the ADC linearity and noise.
- Reduce the ADC power and settling/current requirements on the input signal and references.

Next Tapeout Date: March 2019.