15 bit, 1MS/sec, 2nd Order Noise Shaped SAR ADC

Abstract:

Since the introduction of 90nm CMOS Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However the best performing ADCs from a power consumption point of view have 10bits of resolution and a signal bandwidth of <1MHz. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic which all benefit from faster CMOS technologies. This work aims to leverage this speed advantage through oversampling and noise shaping to achieve an ADC with greater precision.

Introduction

The most efficient ADCs are limited by thermal noise. The comparator adds thermal noise and the faster the SAR ADC the larger the comparator noise bandwidth and its total integrated noise. The first Panther ADC chip consisted of a 10 bit SAR core, a noise shaping loop filter use duty cycled open loop trans-conductance (GM) stages as integrators and a summing comparator. The performance of this ADC was limited by the wideband thermal noise of the GM stages and the fact that the integrators were designed for a fixed clock frequency.

Target Specifications:

Specification Name	Typical	Description
Sampling rate	75MS/s	rate at which input signal is sample 2ns S&H time
SAR clock rate (synchronous)	1.5GS/s	Synchronous timing uses an external clock
Resolution w/o shaping	10ENOB	resolution of SAR core 10bits + 2 redundant bits
Input signal bandwidth	1MHz	target signal frequency
Resolution with shaping	15ENOB	Target resolution for shaped ADC
SNDR @100kHz	90dB	Target resolution for signals at 1MHz
Supply voltage	0.9V	Use core supply if possible to reduce number of supply pins
Power	<5 mW	Power to create a competitive FoM

ADC Architecture and Model:

For the Panther2 ADC an error feedback topology had been implemented. The error feedback topology samples the residue at the end of one conversion and creates a gained version of the residue on a capacitor. This gained residue is capacitively subtracted from the next sampled value of the ADC input. A first order feedback filter has been used as this has the lowest circuit thermal noise. The residue sample and gain circuit uses a dynamic amplifier gain stage which allows the loop filter thermal noise and power consumption to be reduced. Self-timing is added to the dynamic amplifiers to allow the loop filter to operate independently to the ADC rate.

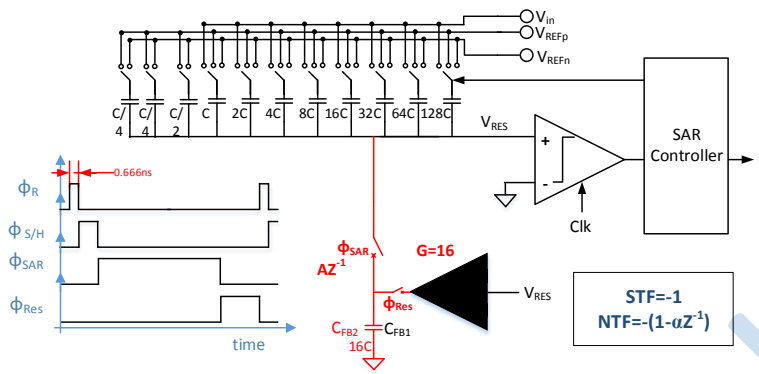

Figure 1: ADC Architecture with the Error Feedback topology

Identified improvements:

Based on the Panther2 measured results the team identified that the following improvements were required.

- Fix Capacitor array INL errors.
- Improve linearity of input signal sampling.
- Add chopping to reduce flicker noise from the dynamic amplifier
- Simplify the error feedback amplifier and remove switches.
- Add shaped dither to randomise errors.
- Add additional digital test modes for diagnosis.

These schematic and layout improvements were implemented in Panther2 revision 2. Extracted simulations were run to demonstrate the performance improvement.

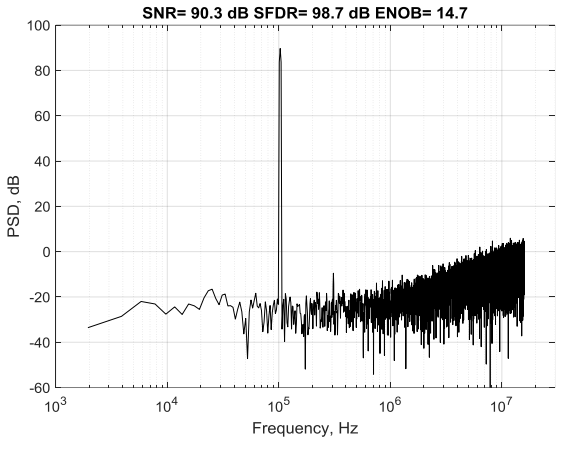

Figure 2(a): transient noise simulation with Dynamic amplifier

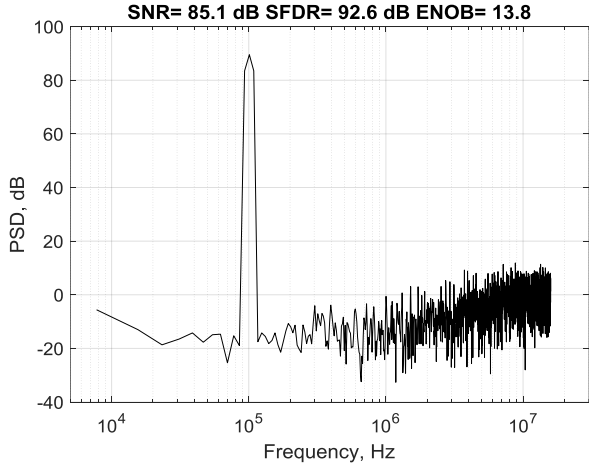

Figure 2(b): SINAD simulation with Extracted dynamic amplifier and chopping

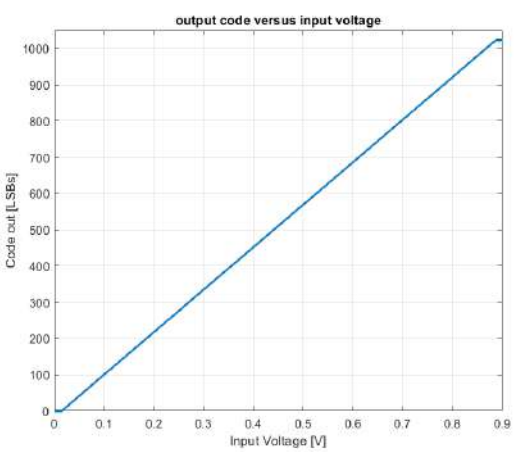

Figure 3(a): PEX ramp results (4 hit per code)

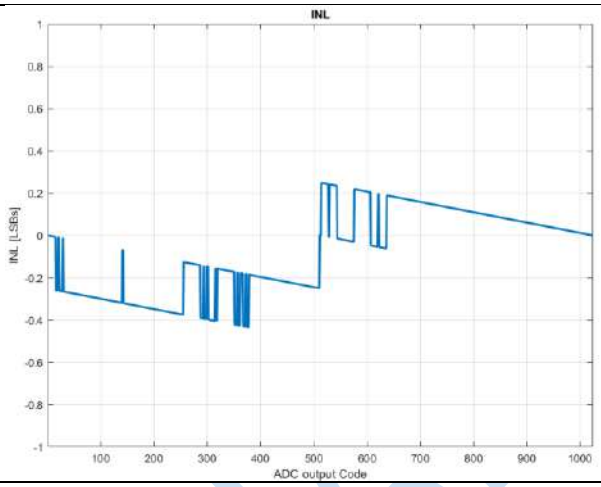

Figure 3(b): PEX ramp INL results

The ADC hierarchy was changed to introduce an analogue Core level. This level contains the key analogue circuits SAR capacitor array, switches, comparator and dynamic amplifier and interconnect. We can simulate this level to make sure that the inter-connect doesn't limit ADC performance. Previously we had difficulty running this simulation as the toplevel contained the digital state machine controller and extracting layout created many extra nodes for the simulator to solve. With multi-core simulations on a multi-core PC we can run 1024 point simulations in under 24 hours. Figure 4(b) shows the ADC all analogue nets toplevel extracted simulation run for 4096 points. This simulation is less than our desired performance but the harmonics that limit the performance are due to systematic capacitor bank errors. These errors can be reduced using on chip calibration or DEM.

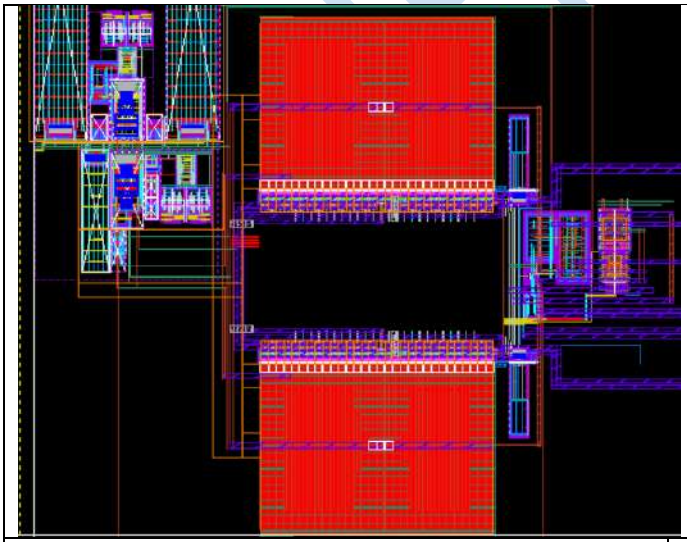

Figure 4(a): Analogue Core layout

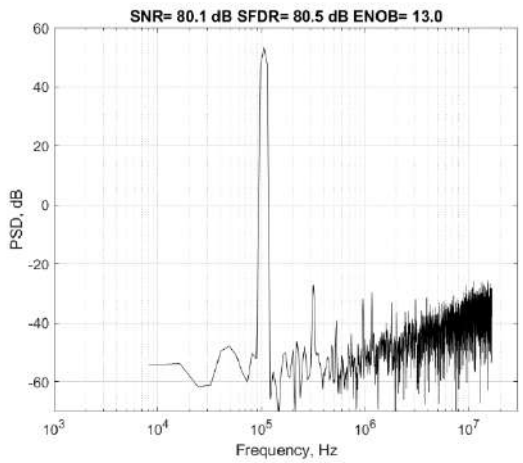

Figure 4(b): PEX analogue core 4096 samples FFT

Summary

Panther2 revision 2 chip has taped out. Chip toplevel extracted simulations show SNR of almost 90dB and SFDR or 81dB. We are verifying in extracted simulations that calibration and DEM can improve the ADC SFDR to the desired 85dB level.

Next Steps:

- Continue running toplevel extracted simulation to demonstrate that calibration can improve performance.
- Prepare for testing.
- Measure the panther2v2 chip performance and submit publications.