15 bit, 2nd Order Noise Shaped SAR @ 1MS/sec

Abstract:

Since the introduction of 90nm CMOS Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However the best performing ADCs from a power consumption point of view have 10bits of resolution and a signal bandwidth of <1MHz. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic which all benefit from faster CMOS technologies. This work aims to leverage this speed advantage through oversampling and noise shaping to achieve an ADC with greater precision.

Introduction

The most efficient ADCs are limited by thermal noise. The comparator adds thermal noise and the faster the SAR ADC the larger the comparator noise bandwidth and its total integrated noise. The first Panther ADC chip consisted of a 10 bit SAR core, a noise shaping loop filter use duty cycled open loop trans-conductance (GM) stages as integrators and a summing comparator. The performance of this ADC was limited by the wideband thermal noise of the GM stages and the fact that the integrators were designed for a fixed clock frequency.

Target Specifications:

Specification Name	Typical	Description
Sampling rate	75MS/s	rate at which input signal is sample 2ns S&H time
SAR clock rate (synchronous)	1.5GS/s	Synchronous timing uses an external clock
Resolution w/o shaping	10ENOB	resolution of SAR core 10bits + 2 redundant bits
Input signal bandwidth	1MHz	target signal frequency
Resolution with shaping	15ENOB	Target resolution for shaped ADC
SNDR @100kHz	90dB	Target resolution for signals at 1MHz
Supply voltage	0.9V	Use core supply if possible to reduce number of supply pins
Power	<5 mW	Power to create a competitive FoM

ADC Architecture and Model:

For the Panther2 ADC an error feedback topology had been implemented. The error feedback topology samples the residue at the end of one conversion and creates a gained version of the residue on a capacitor. This gained residue is capacitively subtracted from the next sampled value

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of the ADC input. A first order feedback filter has been used as this has the lowest circuit thermal noise. The residue sample and gain circuit uses a dynamic amplifier gain stage which allows the loop filter thermal noise and power consumption to be reduced. Self-timing is added to the dynamic amplifiers to allow the loop filter to operate independently to the ADC rate.

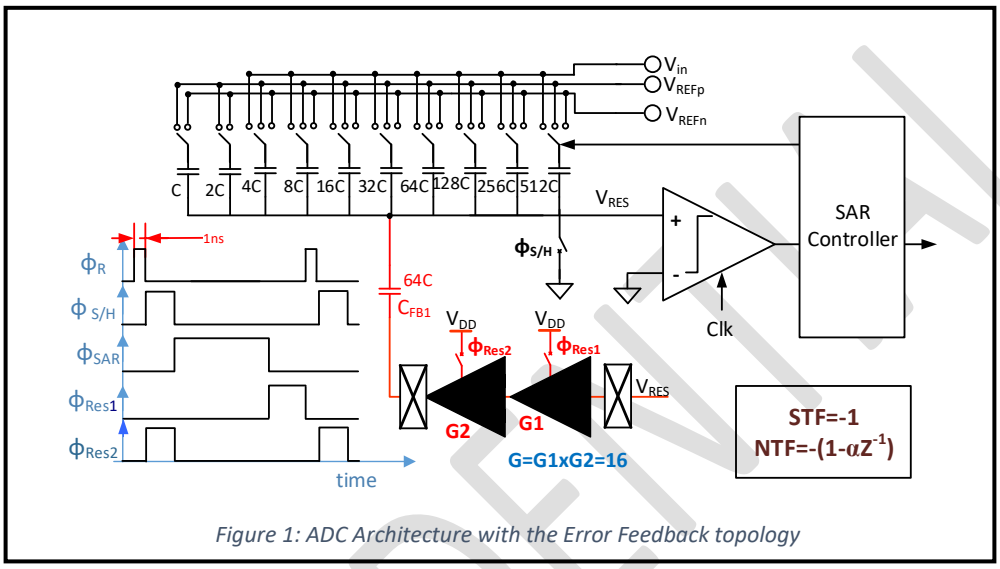

Figure 1: ADC Architecture with the Error Feedback topology

Panther2v3 testing:

Panther2 revision 3 Silicon has arrived back. Initial testing has just started. Five of the 6 assembly boards are functional which is an improvement on previous PCB assembly. We have taken some initial measurements but calibrations and parameter sweeps still need to be performed. Fig. 2 shows measured INL results and an SINAD plot of the SAR core without noise shaping. The INL results still show mismatch between the MSB capacitor and the LSBs and a repeated pattern every 64 codes due to mismatch between the segmented MSBs and the binary weighted LSBs. Extra dummies and shielding have been added on this version. The SINAD plot shows good SFDR performance for the SAR core

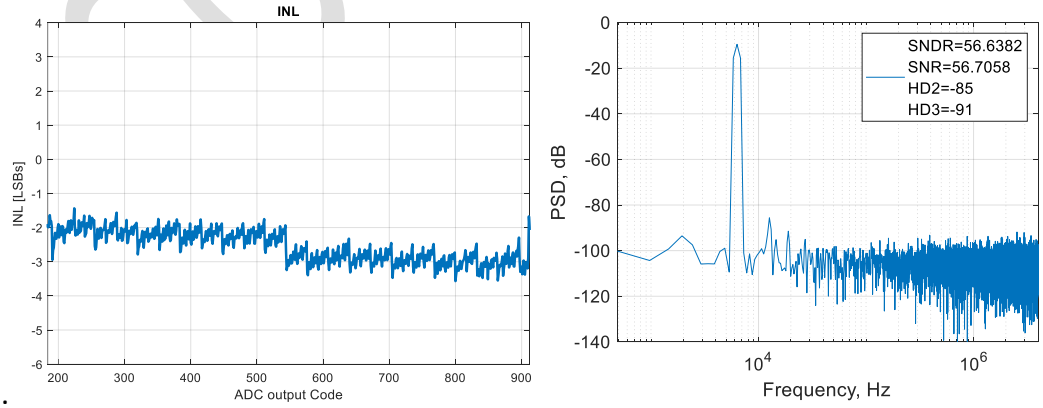

Figure 2: Measured Results from Panther 2v3

Panther3 a new noise shaping topology:

Work on a new noise shaping topology is ongoing. This topology will implement 2nd order shaping and allow the core SAR resolution to be reduced to 6bits. Fig.3 shows a SINAD plot demonstrating second order shaping. Further work is still ongoing to achieve better SINAD and to make sure the linearity of the ADC is not impacted by the larger residue voltages that are due to the reduced SAR resolution.

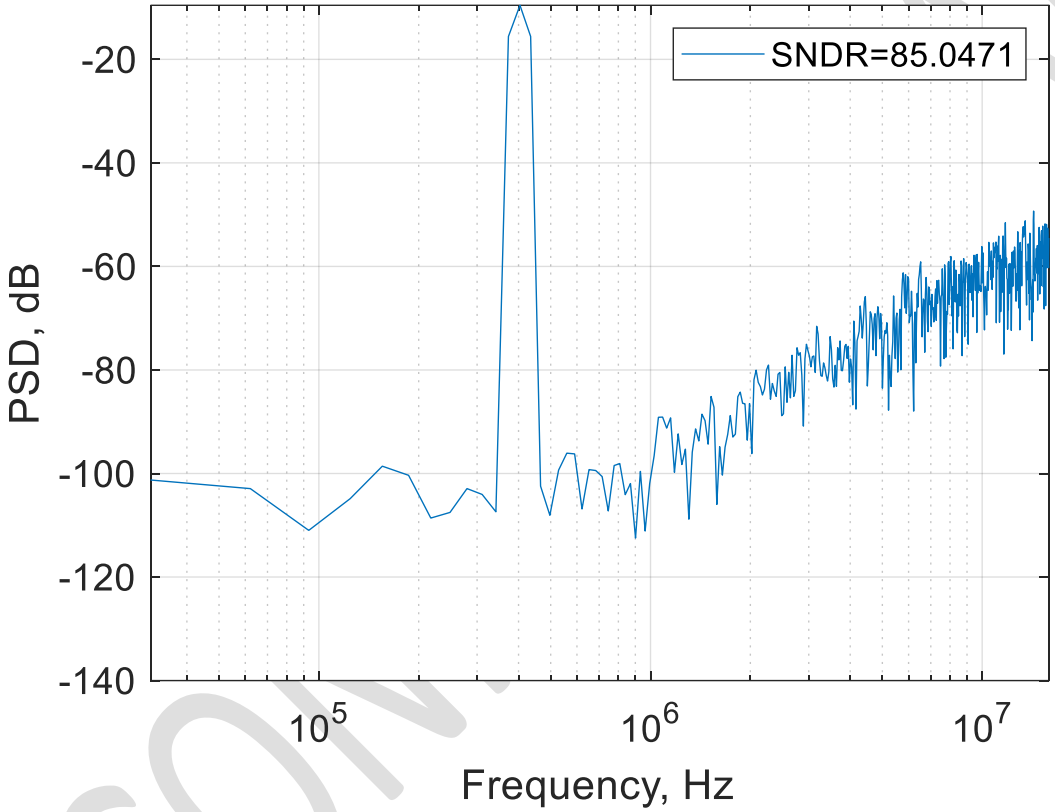

Figure 3: Simulated results of new architecture

Summary

Testing of Panther2v3 and design of Panther3 are ongoing.

Next Steps:

- Testing of Panther2v3 silicon parts.
- Panther 3 is preparing for a tapeout in May 2021.

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