15 bit, 2nd Order Noise Shaped SAR @ 1MS/sec

Abstract:

Since the introduction of 90nm CMOS Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However the best performing ADCs from a power consumption point of view have 10bits of resolution and a signal bandwidth of <1MHz. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic which all benefit from faster CMOS technologies. This work aims to leverage this speed advantage through oversampling and noise shaping to achieve an ADC with greater precision.

Introduction

The most efficient ADCs are limited by thermal noise. The comparator adds thermal noise and the faster the SAR ADC the larger the comparator noise bandwidth and its total integrated noise. The first Panther ADC chip consisted of a 10 bit SAR core, a noise shaping loop filter use duty cycled open loop trans-conductance (GM) stages as integrators and a summing comparator. The performance of this ADC was limited by the wideband thermal noise of the GM stages and the fact that the integrators were designed for a fixed clock frequency.

Target Specifications:

Specification Name	Typical	Description
Sampling rate	75MS/s	rate at which input signal is sample 2ns S&H time
SAR clock rate (synchronous)	1.5GS/s	Synchronous timing uses an external clock
Resolution w/o shaping	10ENOB	resolution of SAR core 10bits + 2 redundant bits
Input signal bandwidth	1MHz	target signal frequency
Resolution with shaping	15ENOB	Target resolution for shaped ADC
SNDR @100kHz	90dB	Target resolution for signals at 1MHz
Supply voltage	0.9V	Use core supply if possible to reduce number of supply pins
Power	<5 mW	Power to create a competitive FoM

ADC Architecture and Model:

For the Panther2 ADC an error feedback topology had been implemented. The error feedback topology samples the residue at the end of one conversion and creates a gained version of the residue on a capacitor. This gained residue is capacitively subtracted from the next sampled value of the ADC input. A first order feedback filter has been used as this has the lowest circuit thermal noise. The residue sample and gain circuit uses a dynamic amplifier gain stage which allows the

loop filter thermal noise and power consumption to be reduced. Self-timing is added to the dynamic amplifiers to allow the loop filter to operate independently to the ADC rate.

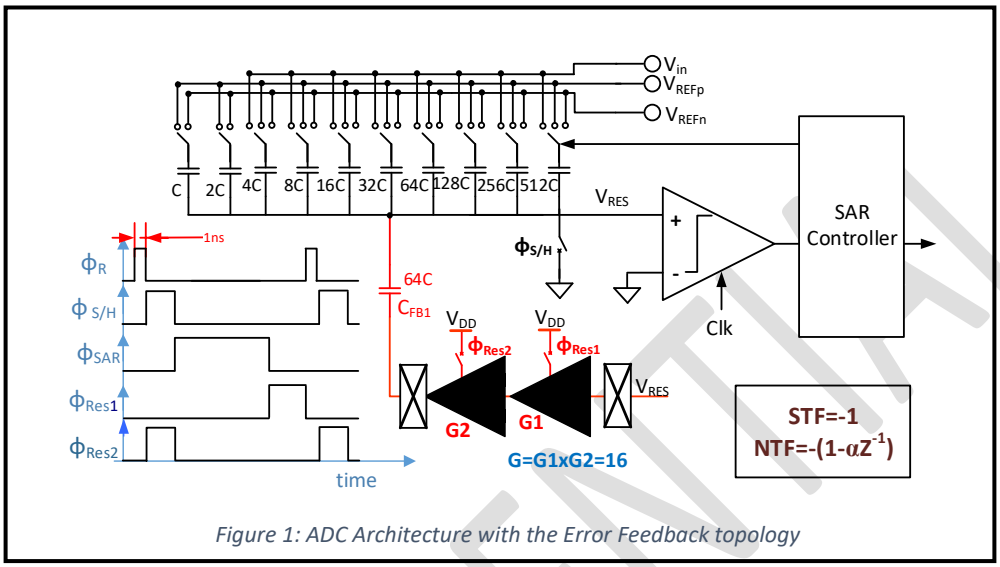

Figure 1: ADC Architecture with the Error Feedback topology

Identified improvements:

Based on the Panther2 measured results the team identified that the following improvements were required.

- Fix Capacitor array INL errors.
- Improve linearity of input signal sampling.
- Add chopping to reduce flicker noise from the dynamic amplifier
- Simplify the error feedback amplifier and remove switches.
- Add shaped dither to randomise errors.
- Add additional digital test modes for diagnosis.

These schematic and layout improvements were implemented in Panther2 revision 2. Extracted simulations were run to demonstrate the performance improvement.

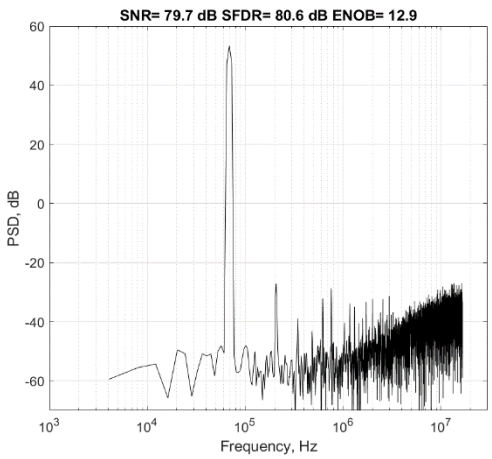

Figure 2(a): SINAD transient noise simulation with extracted ADC before calibration

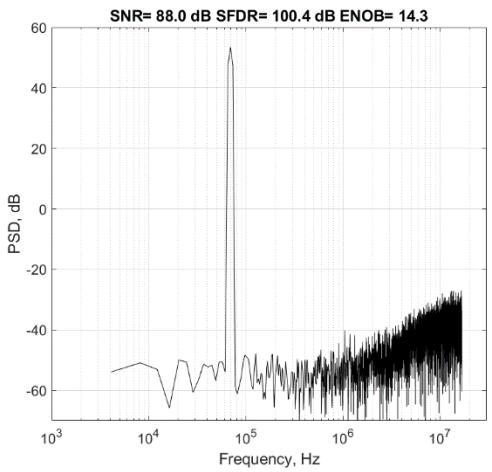

Figure 2(b): SINAD transient noise simulation with extracted ADC after calibration

Measured Results:

Due to Covid-19 we used an external contractor to bump the die and attach them to our PCB. The external contractor had bonding machine fault which delayed PCBs with die until September.

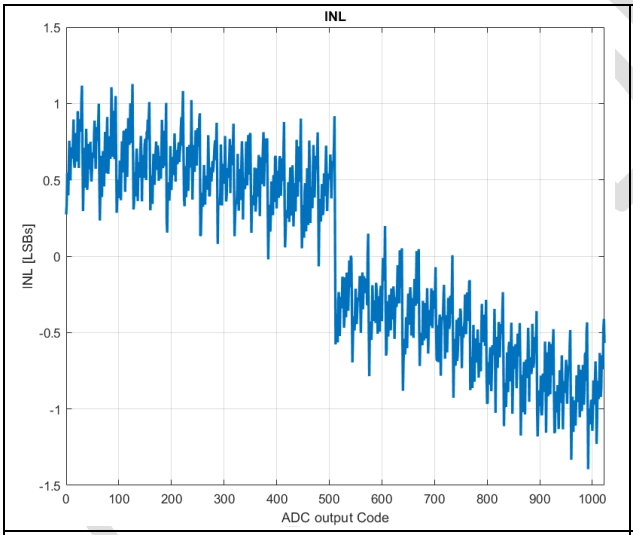

Figure 3(a): INL results part B5 shuffle state 0

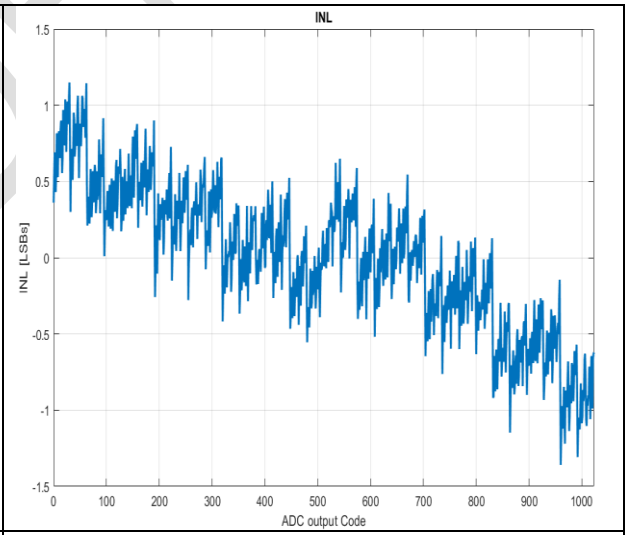

Figure3(b): INL results part B5 shuffle state 2

Ramp tests have been run on the 10bit SAR Core to quantify the performance. Despite improvements made to the layout and good extracted simulation results a step is still seen in the INL plots at the MSB transition. In Fig. 3(a) the MSB capacitors are on the left and right extremities of the capacitor array. Using the manual shuffle digital feature the MSB capacitors can be moved away from the extremities. Fig. 3(b) shows the INL result for this case. Chemical mechanical polishing (CMP) is a possible cause of the mismatch, we recommend adding more dummies to capacitor arrays in 28nm. The INL results also show a sawtooth pattern every 32 codes due to mismatch between the MSB columns and LSBs. This is a similar characteristic to Panther2.

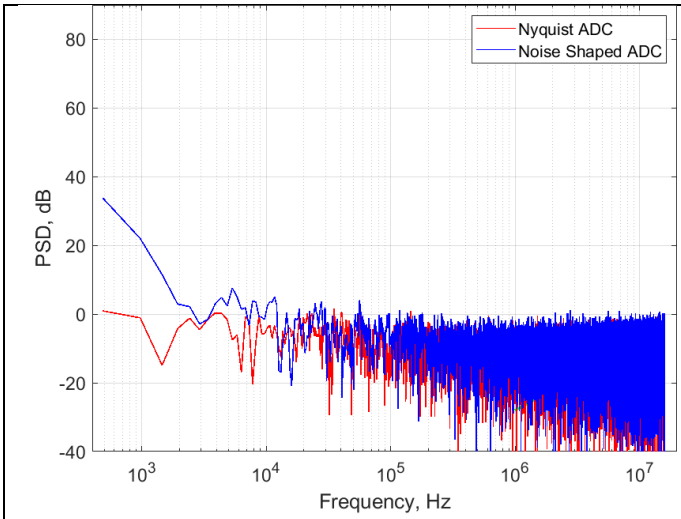

Figure 4(a): SNR of ADC with no signal with and without NS

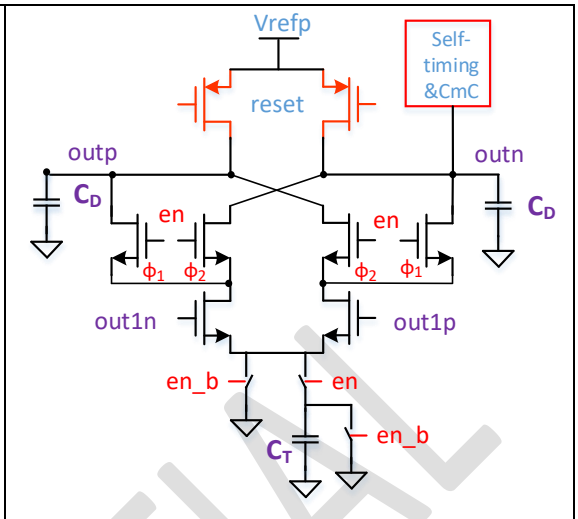

Figure 4(b): 2nd Dynamic amplifier stage

SINAD tests with noise shaping enabled are not functioning correctly. Current consumption with noise shaping enabled shows a change in current consumption on the Vrefp pin of less that 1uA compared to noise shaping turned off. The expected current consumption is 6uA. Debugging is on-going but a possible cause is that the Pmos devices in Fig. 4 (b) have been damaged and are not resetting the Dynamic amplifier correctly. These devices are minimum sized. ESD is a potential source – experiments are ongoing to prove/disprove this theory. 3 of the 4 parts tested exhibit the same behavior.

Summary

Panther2 revision 2 testing is on-going. Noise shaping is not operating correctly. De-bug is on-going to find the cause of the problem.

Next Steps:

- De-bug noise shaping failures
- Design a wire-bond board as this would avoid potential ESD problems and allow possible FIB experiments to be carried out and tested.