15 bit, 2nd Order Noise Shaped SAR @ 1MS/sec

Abstract:

Since the introduction of 90nm CMOS Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However the best performing ADCs from a power consumption point of view have 10bits of resolution and a signal bandwidth of <1MHz. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic which all benefit from faster CMOS technologies. This work aims to leverage this speed advantage through oversampling and noise shaping to achieve an ADC with greater precision.

Introduction

The most efficient ADCs are limited by thermal noise. The comparator adds thermal noise and the faster the SAR ADC the larger the comparator noise bandwidth and its total integrated noise. The first Panther ADC chip consisted of a 10 bit SAR core, a noise shaping loop filter use duty cycled open loop trans-conductance (GM) stages as integrators and a summing comparator. The performance of this ADC was limited by the wideband thermal noise of the GM stages and the fact that the integrators were designed for a fixed clock frequency.

Target Specifications:

Specification Name	Typical	Description
Sampling rate	75MS/s	rate at which input signal is sample 2ns S&H time
SAR clock rate (synchronous)	1.5GS/s	Synchronous timing uses an external clock
Resolution w/o shaping	10ENOB	resolution of SAR core 10bits + 2 redundant bits
Input signal bandwidth	1MHz	target signal frequency
Resolution with shaping	15ENOB	Target resolution for shaped ADC
SNDR @100kHz	90dB	Target resolution for signals at 1MHz
Supply voltage	0.9V	Use core supply if possible to reduce number of supply pins
Power	<5 mW	Power to create a competitive FoM

ADC Architecture and Model:

For the Panther2 ADC an error feedback topology had been implemented. The error feedback topology samples the residue at the end of one conversion and creates a gained version of the residue on a capacitor. This gained residue is capacitively subtracted from the next sampled value of the ADC input. A first order feedback filter has been used as this has the lowest circuit thermal

noise. The residue sample and gain circuit uses a dynamic amplifier gain stage which allows the loop filter thermal noise and power consumption to be reduced. Self-timing is added to the dynamic amplifiers to allow the loop filter to operate independently to the ADC rate.

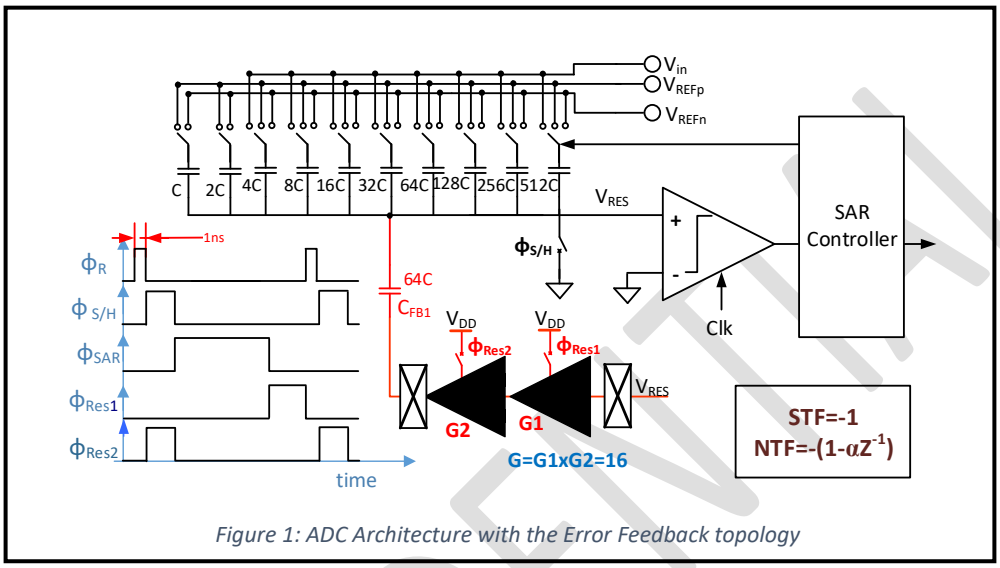


Figure 1: ADC Architecture with the Error Feedback topology

Panther2v3 improvements:

A version of panther was taped out at the end of October making 3 modifications. SINAD tests with noise shaping enabled on Panther2v2 (Fig. 3(a)) were not functioning correctly. Current consumption with noise shaping enabled showed a change in current consumption on the Vrefp pin of less that 1uA compared to noise shaping turned off. The expected current consumption is 6uA. Debugging is on-going but a possible cause is that the Pmos devices in Fig. 3 (b) have been damaged and are not resetting the Dynamic amplifier correctly. On Panther2v3 these devices were replaced with larger switches.

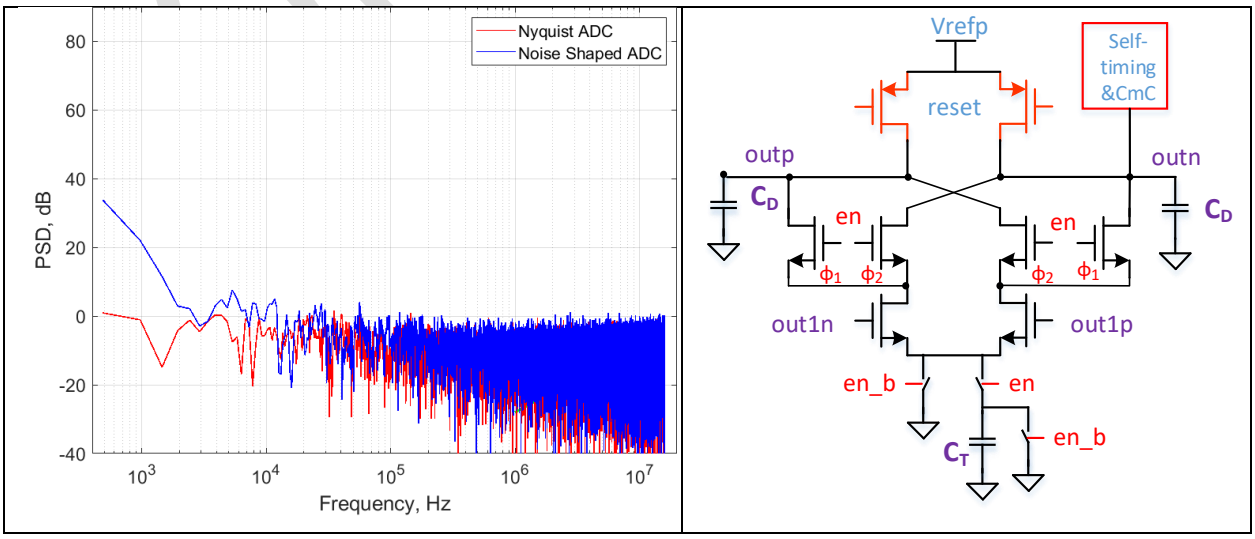
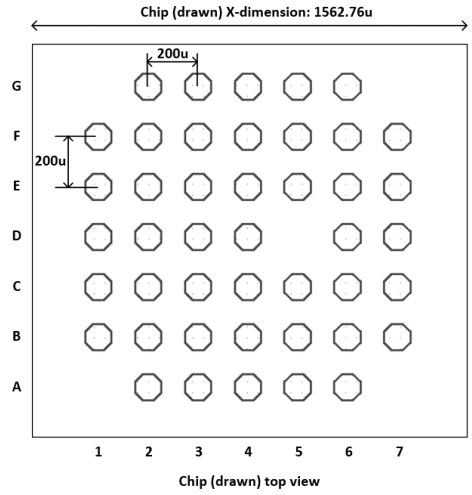


Figure 3(a): SNR of ADC with no signal with and without NS	Figure 3(b): 2nd Dynamic amplifier stage

Further changes made were the addition of extra dummy capacitors around the Capacitor array to see if this improves capacitor matching. The total number of chip pins from the chip was also reduced enabling a 200um pitch to be used for the output pads. Earlier versions of panther required a custom wirebond process to add solder bumps to the bare die before they were attached to the PCBs. The larger pitch now used allows the standard bumping process from IMEC to be used to add bumps to the bare die. Fig. 4 shows the new output pin configuration.



Chip top view: Pin names

	DVDD_IO_1P8	VSS_DIG_SAR	DMISC	AVDD_NS	AVSS_NS	
SDA	DVDD_IO_0P9	VDD_DIG_SAR	AVSS_IO	AVDD_SAR	AVSS_SAR	AMISC
SCL						VINP
DVSS_IO	DVSS_IO				VCM1	VINN
DVDD_IO_1P8				AVSS_CLK	AVDD_CLK	CLKP
DVDD_IO_0P9	RESET	AVSS_IO	Vrefn_1	AVDD_VREF	AVDD_CLK1P8	CLKN
	DVSS_IO	AVDD_IO_1P8	Vrefp_1	Vrefp_2	AVSS_VREF	

Figure 4: Reduced output pins allowing 200um pitch

Publications: A journal paper on "Recent Advances and Trends in Noise Shaping SAR ADCs" was accepted for publication in the IEEE journal Transactions on Circuits and Systems II. This paper overview of NS-SAR architectures with some predictions for future trends. It will be published in the January 2021 journal. A pre-published copy is attached.

Summary

Panther2 revision 3 was taped out to solve issues with the previous part. Silicon is due back at end of February. Work on a new noise shaping topology has started and it is hoped to tapeout a silicon demonstrator in May 2021. A journal paper "Recent Advances and Trends in Noise Shaping SAR ADCs" has been accepted for publication.

Next Steps:

- Testing of Panther2v3 silicon parts.
- Implement a new noise shaped topology for Panther 3 and prepare for a tapeout in May 2021.