15 bit, 2nd Order Noise Shaped SAR @ 1MS/sec

Abstract:

Since the introduction of 90nm CMOS Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However the best performing ADCs from a power consumption point of view have 10bits of resolution and a signal bandwidth of <1MHz. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic which all benefit from faster CMOS technologies. This work aims to leverage this speed advantage through oversampling and noise shaping to achieve an ADC with greater precision.

Introduction

The most efficient ADCs are limited by thermal noise. The comparator adds thermal noise and the faster the SAR ADC the larger the comparator noise bandwidth and its total integrated noise. The first Panther ADC chip consisted of a 10 bit SAR core, a noise shaping loop filter use duty cycled open loop trans-conductance (GM) stages as integrators and a summing comparator. The performance of this ADC was limited by the wideband thermal noise of the GM stages and the fact that the integrators were designed for a fixed clock frequency.

Target Specifications:

Specification Name	Typical	Description
Sampling rate	75MS/s	rate at which input signal is sample 2ns S&H time
SAR clock rate (synchronous)	1.5GS/s	Synchronous timing uses an external clock
Resolution w/o shaping	10ENOB	resolution of SAR core 10bits + 2 redundant bits
Input signal bandwidth	1MHz	target signal frequency
Resolution with shaping	15ENOB	Target resolution for shaped ADC
SNDR @100kHz	90dB	Target resolution for signals at 1MHz
Supply voltage	0.9V	Use core supply if possible to reduce number of supply pins
Power	<5 mW	Power to create a competitive FoM

ADC Architecture and Model:

For the Panther2 ADC an error feedback topology had been implemented. The error feedback topology samples the residue at the end of one conversion and creates a gained version of the residue on a capacitor. This gained residue is capacitively subtracted from the next sampled value of the ADC input. A first order feedback filter has been used as this has the lowest circuit thermal noise. The residue sample and gain circuit uses a dynamic amplifier gain stage which allows the loop filter thermal noise and power consumption to be reduced. Self-timing is added to the dynamic amplifiers to allow the loop filter to operate independently to the ADC rate.

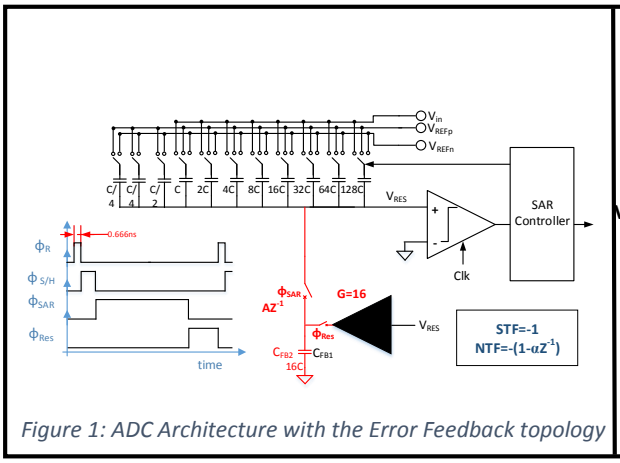

Figure 1: ADC Architecture with the Error Feedback topology

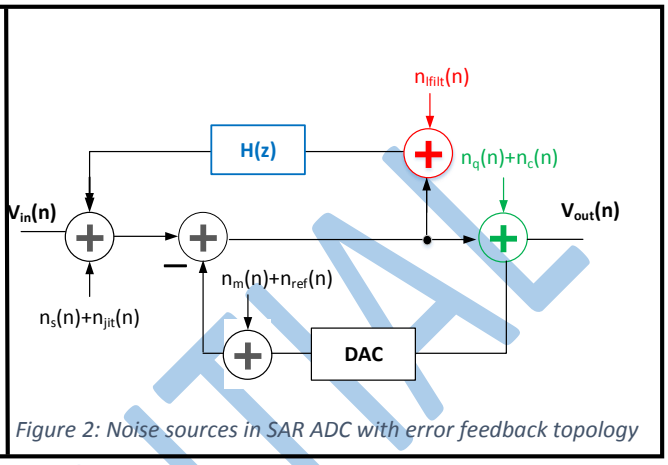

Figure 2: Noise sources in SAR ADC with error feedback topology

Simulation Results:

Simulation results are shown in Figures 3,4 and 5. Figure 3 shows schematic simulations with transient noise. This result demonstrates the target specifications. Figure 4 shows a C only top-level simulation of the ADC without transient noise using a parasitic extracted model of the capacitor array and switches. This simulation shows some distortion reducing the ADC performance. Figure 5 shows a top-level simulation at a lower rate 35MS/s with transient noise using an extracted model of the capacitor array and switches. This simulation is limited by distortion.

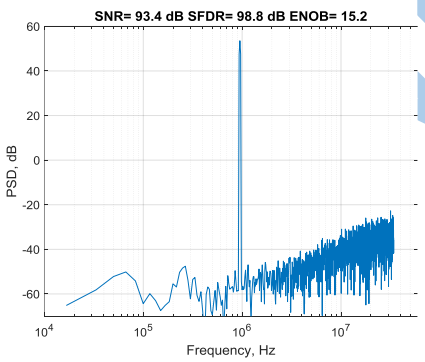

Figure 3: Top-level schematic simulation with transient noise.

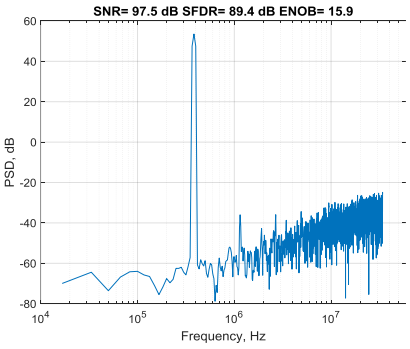

Figure 4: Top-level sim Extracted C-array switches no transient noise 70MS/s rate.

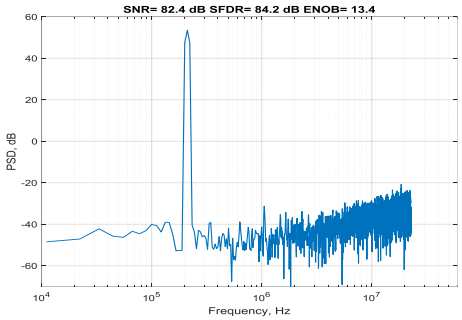

Figure 5: Top-level sim Extracted C-array switches (R&C) transient noise 35MS/s rate

Measured Results:

Measured SINAD results are shown in Figures 6 and 7. Both of these plots display lots of harmonics. The causes of this distortion is attributed to the input sampling network of the ADC and the PCB input network. Flicker noise is displayed in both plots, this was not seen in simulation as simulations with more than 4096 FFT points could not be run. Of more concern is the higher than expected noise floor after the flicker noise rolls off. This is not expected and it been investigated at present. These are results after one month of testing and debug is ongoing to investigate the causes of the degradation of performance from simulation.

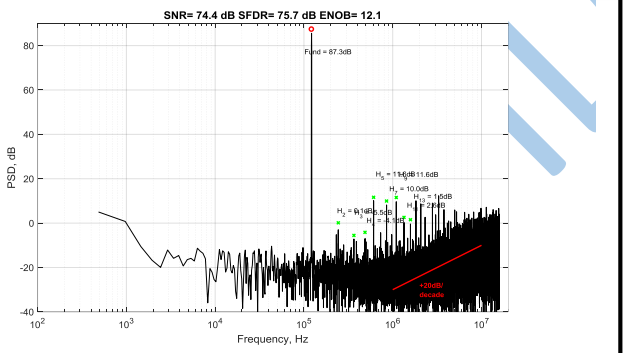

Figure 6: Measurement for 121kHz tone with ADC rate of 32MS/s.

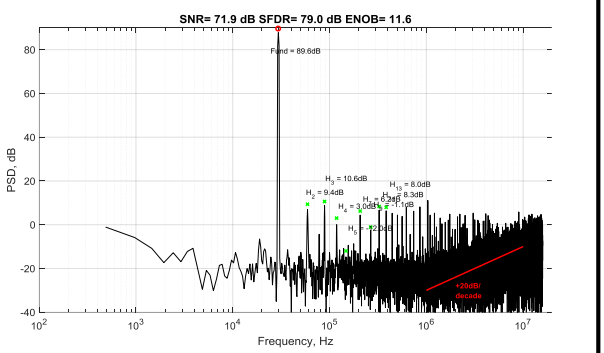

Figure 7: Measurement for 30kHz tone with ADC rate of 32MS/s.

Summary

Functional Silicon with noise shaping has been achieved. However the ADC performance is not meeting expectations. Debug simulations and measurements are underway at present to determine the causes of the extra noise and distortion. Once the root causes have been identified they will be fixed on a future tapeout.

Next Steps:

- Investigation of noise and distortion causes.
- Achieve better measurements and submit a paper to CICC.
- Identify circuit fixes to achieve better results.
- Decide the goals for a future tapeout.

Next Tapeout Date: March 2020 (TBC).