Ultra-low Power Sensor interface for Biomedical Application

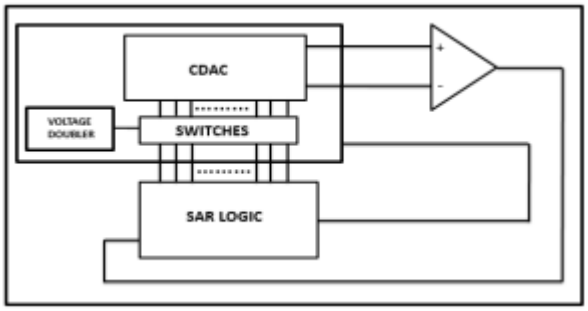
Abstract:

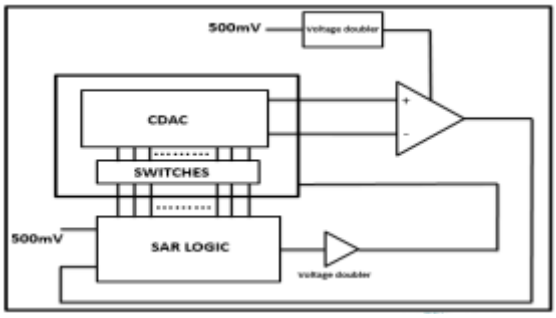
Successive Approximation Register (SAR) ADCs have become the dominant low power high resolution ADC architecture. This paper presents a 14-bit SAR ADC for biomedical applications. It is not obvious to maintain good power efficiency for medium resolution, low data rate ADC'S given fixed overhead and scaling limitations, nevertheless, an excellent FOM of 1FJ/Conversion step is achieved by using a voltage boosting technique, synchronous dynamic logic , an optimized layout and reduced power supply. Power Efficient SAR ADCs are limited by the thermal noise contribution from the comparator. One additional bit of resolution when approaching the KT/C noise limit, leads to 4x larger capacitance, with an equivalent increase of power consumption. Therefore, maintaining very low FOM with increasing ENOB is quite challenging and definitely not straightforward.

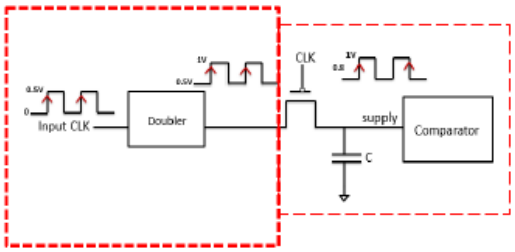
Proposed ADC architecture:

This work aims to reduce the power in a SAR, by reducing the supply voltage from 1.2V in standard 65nm to 0.5V, without reduction in performance. Logic power dominates below 9 bit, analogue power dominates greater than 12 bits. Our approach is to first design each of the blocks with "just" enough power, run the various blocks at the appropriate voltage and eliminate any wasted power. Once each of the blocks are designed for just the power required to make decision, the next step is to employ voltage boosting technique to boost each of the blocks to the optimum voltage required for operation. We have designed a low powered TSPC LOGIC [3] which can operate at 500mV supply, then boost this supply voltage given to logic to required voltage for each of the blocks. This designed TSPC logic consumes approximately 10% lower power than regular TSPC logic. For the comparator design, since it is a power hungry block in this ADC, we want to limit the amount of power consumed by adding a capacitor at the supply of the regular dual tail dynamic comparator.

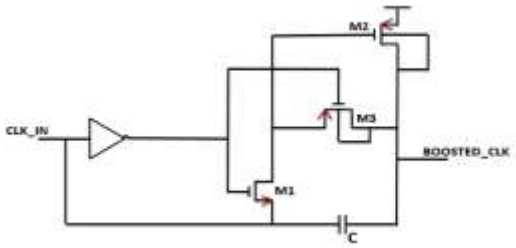
ADC Architecture and Model: (shrew x1 and x2)



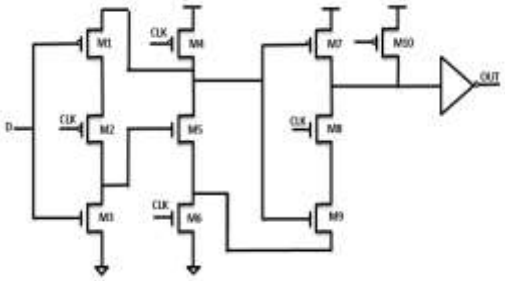




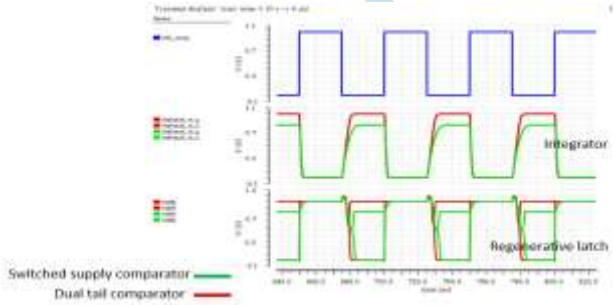
Power supply methodology to the comparator



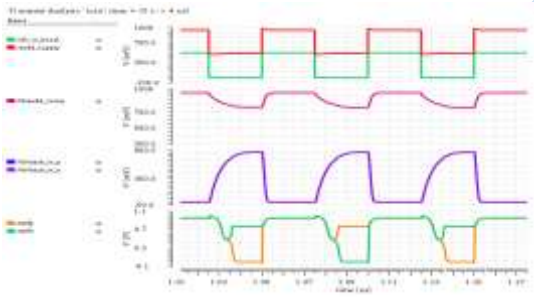
voltage boosting circuit topology



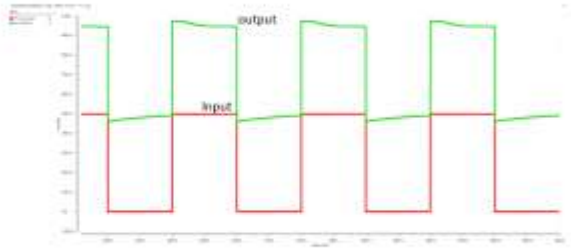
Low powered glitch free TSPC logic



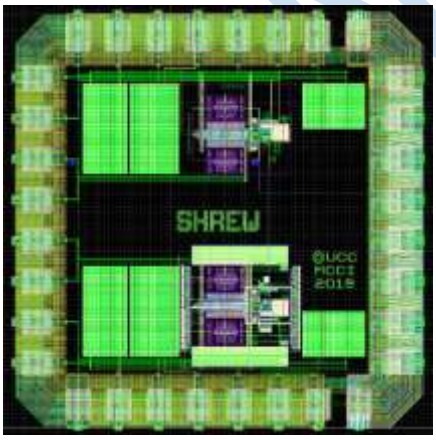
18 % power improvement without FIB, 53 % power improvement with FIB



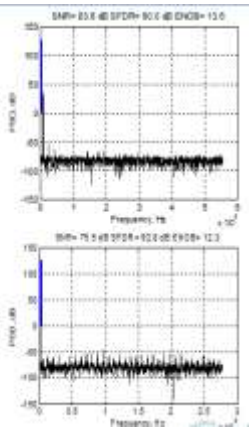
Supply waveform for 500Mv comparator



Comparator Doubler circuit waveform



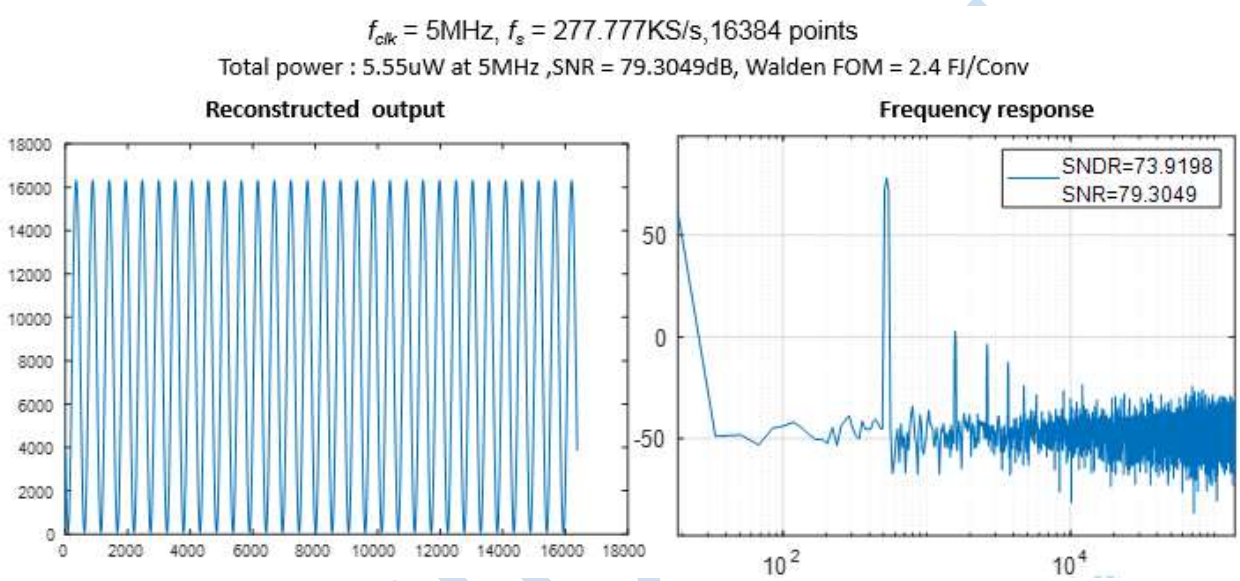
Parameter	SHREW_X2	SHREW_X2 TRANSIENT NOISE
Clk frequency	20MHz	20MHz
Sampling frequency	2MHz	2MHz
ENOB (schematic)	13.6	12.3
SNR	83.6 dB	75.5 dB
SFDR	90.0 dB	92.8 dB
Number of points	4096; M = 31	4096; M = 31
Supply	1V	1V
Vrefp, Vrefn	700mV, 0V	700mV, 0V
Vcm	350m	350m
Input swing	695m to -695m	695m to -695m
Power(uW)	8u	8u
FOM(fJ/C.conv) (extracted)	0.58	0.9



We taped out two architectures. The regular split CDAC array architecture (Shrew X1) is designed with each of the blocks to get maximum performance for the power metric at 1V. In the second version (Shrew

X2), with a reduced supply voltage of 500mV, we are boosting the power supply to the optimum operating voltage of each of the blocks rather than designing the blocks to a lesser supply voltage.

Shrew testing update:
Below are plots for Shrew X1:



We still need to get the INL and DNL plots for version 1. Version 2 is functioning but need to follow up the same procedure as that of version 1 to tabulate the performance metrics.

Future work:

- SAR logic for version 1 needs to be replaced with high Vt transistors to mitigate the leakage current.
- Need to increase the input signal range to get better ENOB (nmos integrator).
- 350m volt ADC with the use of Tripler.
- Remove bridge capacitance.
- Whether to add redundancy.
- Work on alternative solution for majority voting w.r.t to comparator noise.