SHREW

Abstract:

Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However, achieving sub 5fJ/Conv-step is a challenge. This work aims to reduce the power in a SAR, by reducing the supply voltage from 1.2 V in standard 65nm to 0.5V, without any reduction in performance.

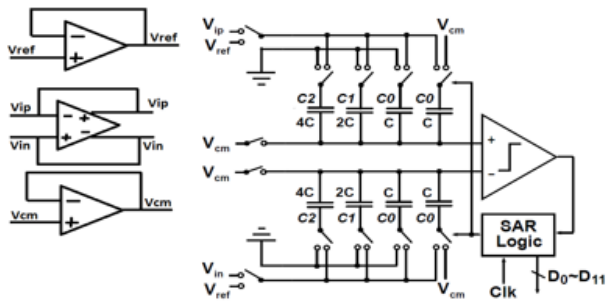
Introduction:

Power Efficient SAR ADCs are limited by the thermal noise contribution from the comparator. This work looks at the reducing the power consumption in the comparator, by reducing the supply voltage from 1.2 V in 65nm to 0.5V. However, most comparator architectures stop working once the supply voltage reduces below approximately 750-800 mV. This research proposes an alternative approach to this challenge.

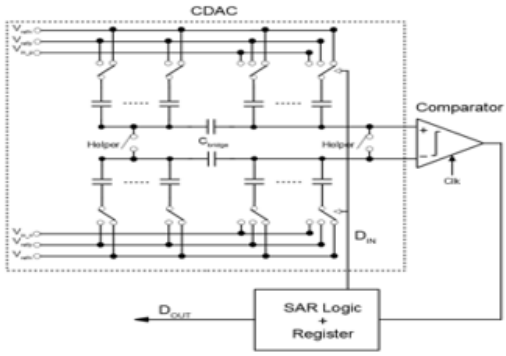
Target Specifications:

CMOS Technology	65nm
Sampling frequency	2MS/s
Resolution	13
Power	<5uW
SNDR	80.02dB
Supply voltage	<1V
FOM(walden)	0.305 (FJ/conversion step)
Input range	+- 1V p-p (2V range)
clock frequency	>28MHz

ADC Architecture and Model:



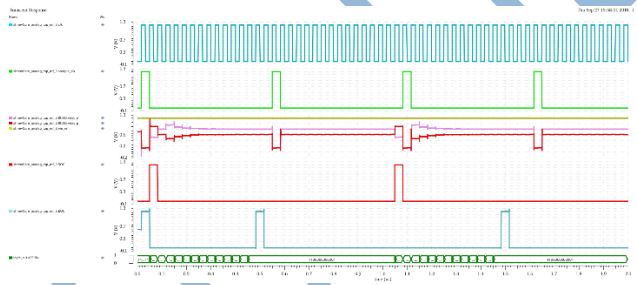
ADC TOP-LEVEL(BINARY WEIGHTED DAC)



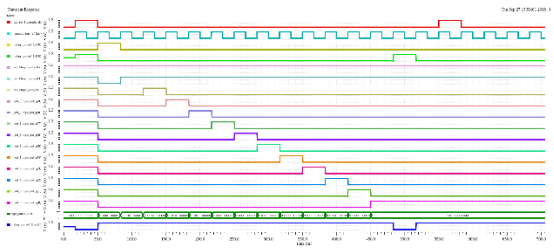
ADC TOP-LEVEL(SPLIT LEVEL DAC)

We plan to tape out with 2 architectures. The split capacitor generally allows low power consumption and a small layout area, however it suffers from low SAR ADC speed. The binary scaled capacitor array allows low unit capacitance and high speed, however, it needs a larger layout area. The split CDAC approach needs much fewer unit cap, but it suffers from higher INL and DNL in comparison with binary scaled counterpart.

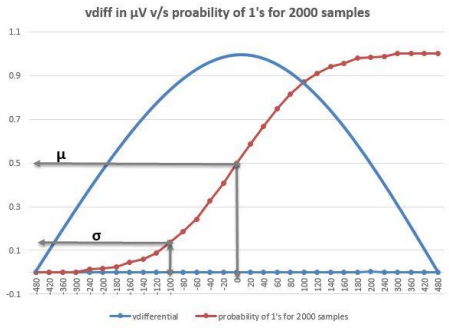
TL schematic Simulation Results:



SCHEMATIC LEVEL SAR ADC OUTPUT WAVEFORM



HAND CRAFTED SAR LOGIC OUTPUT



Thermal noise amplitude distribution will create a cumulative Gaussian probability distribution around the trip level of the comparator decision.

Next Steps:
Comparator layout needs to be modified to add more components (sampling switch at the supply of comparator) and we will then proceed to extracted simulations. Once the analysis of comparator is done, we plan to use the voltage boosting circuit as the power supply for the comparator and test the system.

Tapeout Date: May 2019.