Ultra-low Power Sensor interface for Biomedical Application

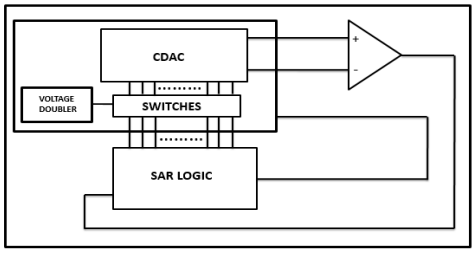
Abstract:

Successive Approximation Register (SAR) ADCs have become the dominant low power high resolution ADC architecture. This paper presents a 14-bit SAR ADC for biomedical applications. It is not obvious to maintain good power efficiency for medium resolution, low data rate ADC'S given fixed overhead and scaling limitations, nevertheless, an excellent FOM of 1FJ/Conversion step is achieved by using a voltage boosting technique, synchronous dynamic logic, an optimized layout and reduced power supply. Power Efficient SAR ADCs are limited by the thermal noise contribution from the comparator. One additional bit of resolution when approaching the KT/C noise limit, leads to 4x larger capacitance, with an equivalent increase of power consumption. Therefore, maintaining very low FOM with increasing ENOB is quite challenging and definitely not straightforward.

Proposed ADC architecture:

This work aims to reduce the power in a SAR, by reducing the supply voltage from 1.2V in standard 65nm to 0.5V, without reduction in performance. Our approach is to first design each of the blocks with "just" enough power, run the various blocks at the appropriate voltage and eliminate any wasted power. Once each of the blocks are designed for just the power required to make decision, the next step is to employ voltage boosting technique to boost each of the blocks to the optimum voltage required for operation. Low powered TSPC LOGIC is designed which can operate at 500mV supply, then boost this supply voltage given to logic to required voltage for each of the blocks. Switched Supply technique is applied to the comparator, while having minimal reduction in performance even when confronted with significant power supply noise.

ADC Architecture and Model: (Shrew x1 and x2)



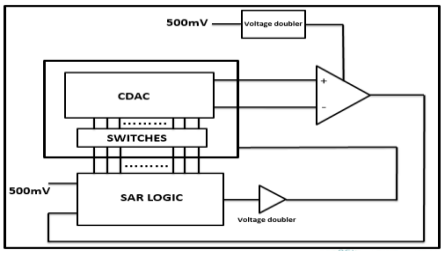


Fig .1. Basic overview Architecture of Shrew x1

Fig .2. Basic overview Architecture of shrew x2

Fig .3 below shows the complete architecture of shrew X1.

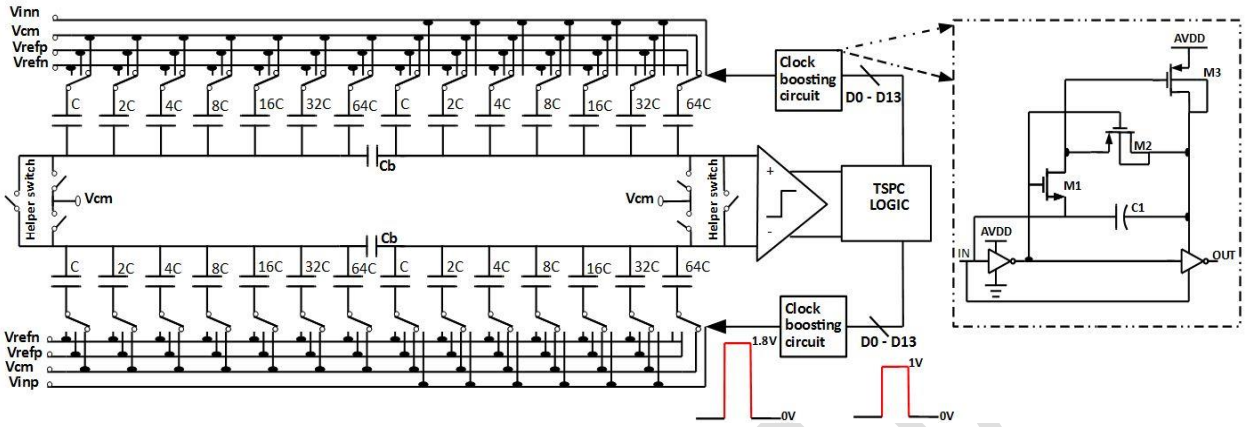


Fig .3. Proposed 14 bit SAR ADC, with Switched Supply comparator, NMOS Clock Boosted driven input sampling switches and hand crafted TSPC logic

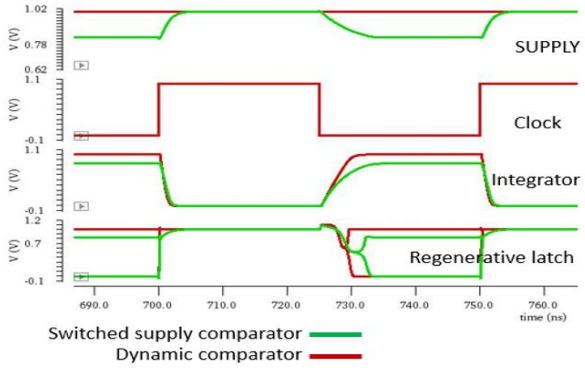


Fig .4. Comparision of proposed and conventional comparator.

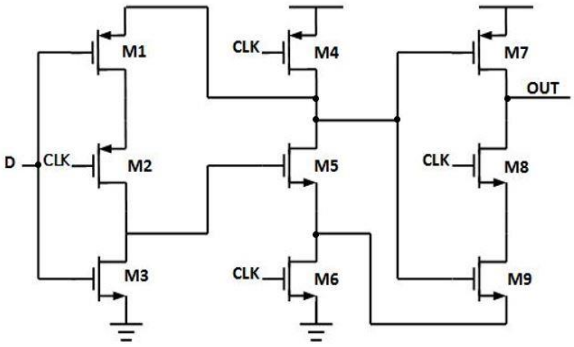


Fig .5. Proposed Low powered TSPC logic

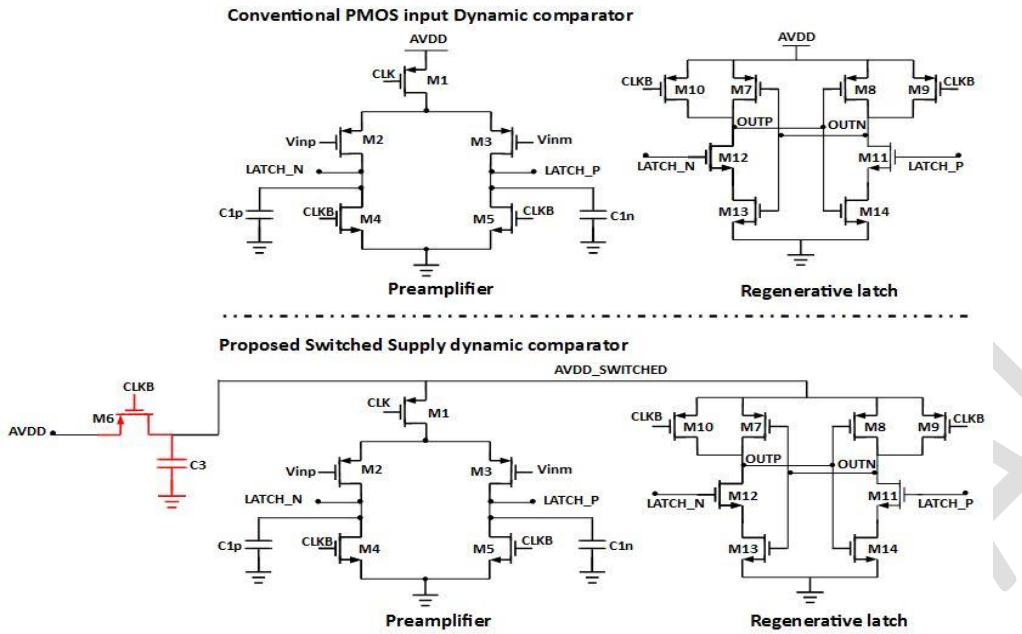


Fig.6. Proposed comparator architecture.

parameter	Shrew x2 (tranisent noise)
Technology	65nm
supply	0.5V
Sample rate (S/s)	1.11M
Resolution	14
ENOB(schematic)	12.3
SNDR(dB)	75.5
Power(W)	8u
FOMw (fJ/conv-step)	1.1
Input sampling	Clock booster

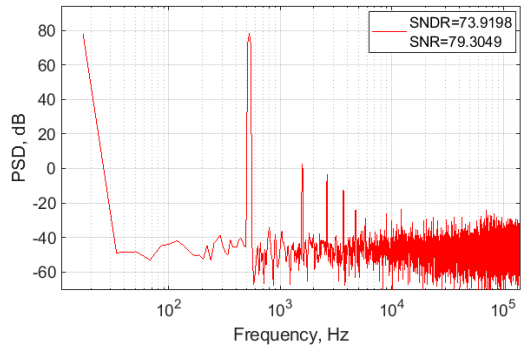
parameter	Shrew x1
Technology	65nm
supply	1V
Sample rate (S/s)	277K
Resolution	14
Power(W)	4.95µ
SNDR(dB)	73.8
FOMw (fJ/conv-step)	4.5
FOMs (dB)	178.3
Input sampling	Clock booster

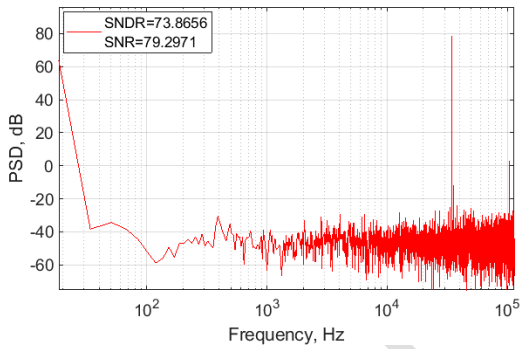
Fig. 7. Performance summary of shrew x1 and Shrew_x2

We taped out two architectures. The regular split CDAC array architecture (Shrew X1) is designed with each of the blocks to get maximum performance for the power metric at 1V. In the second version (Shrew X2), with a reduced supply voltage of 500mV, we are boosting the power supply to the optimum operating voltage of each of the blocks rather than designing the blocks to a lesser supply voltage.

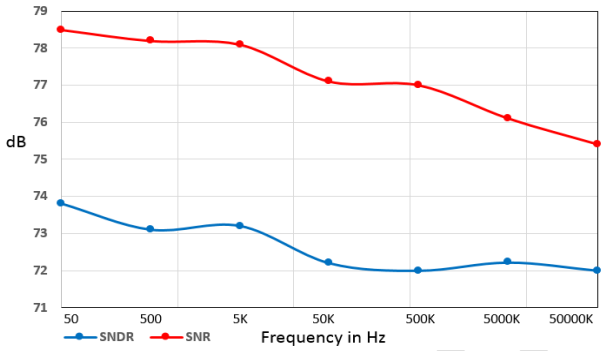
Shrew testing update:

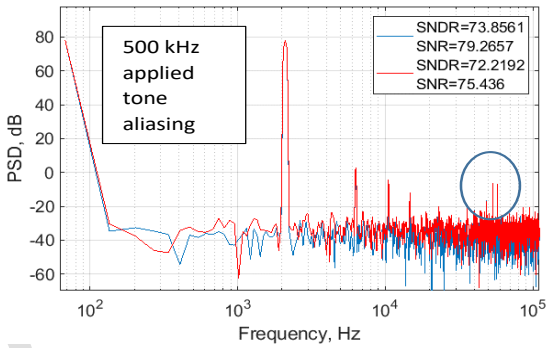
Below are plots for Shrew X1:





16384 output FFT with a 525 Hz input signal on the left and 16384 output FFT with a 35 kHz input signal on the right.

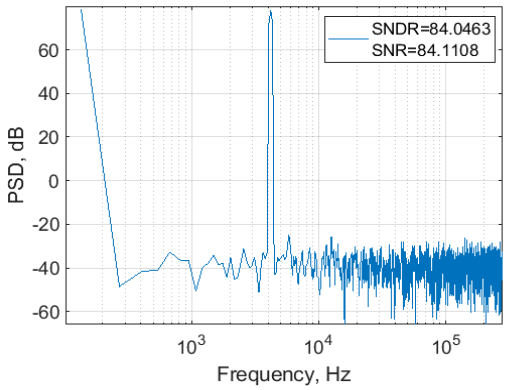




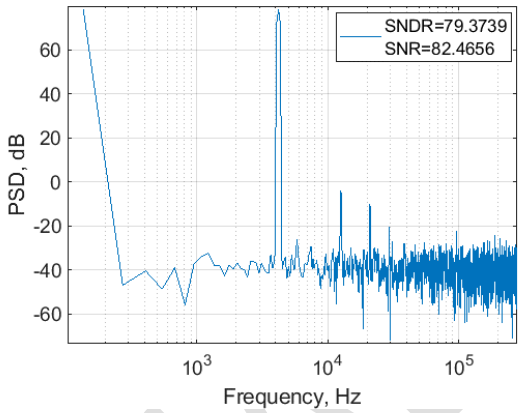
SNDR/SNR versus frequency for a 100 mV tone applied to the Switched Supply comparator with a 1.2 V DC offset, with a 20 kHz input signal applied, and in the right, combination of FFT plot of with (red) supply noise and without (blue) the supply tone at 500 kHz applied.

Shrew_x1_revb Tapeout (Jun 2020):

- Overall architecture remains the same with the addition of control signal block on chip.
- Control signals were given off chip for previous taped out version which resulted in testing issues related to synchronization of clock signal with control signal.
- The ADC was difficult to test at higher clock frequency and to plot the INL and DNL curve due to the synchronization issue. This is now mitigated by generating the control signals on chip.
- Low Vt transistors caused two issues: leakage in the top plate switch and increase in power dissipation. These issue were resolved by using high vt transistors.
- Below are the simulation results showing improvement with the Shrew_x1_revb design changes.



Shrew_x1_revb: supply = 1V;



Shrew_x1: supply = 1V;

- Submitted the paper of shrew x1 to CICC 2021.
- Testing needs to be done for shrew_x1_revb.

Future work:

- **500m volt design, Shrew_x2, has testing issues, and debugging is underway.**
- Include the switching supply methodology to the whole ADC (i.e. switched supply to comparator and sample the reference on the bunch of capacitors).
- Add the switching supply topology to the switching column of capacitor array.