Ultra-low Power Sensor interface for Biomedical Application

Abstract:

Successive Approximation Register (SAR) ADCs have become the dominant low power high resolution ADC architecture. However, achieving sub 1fJ/Conv-step is a challenge. This work aims to reduce the power in a SAR, by reducing the supply voltage from 1.2 V in standard 65nm to 0.5V, without any reduction in performance.

Introduction:

Power Efficient SAR ADCs are limited by the thermal noise contribution from the comparator. One additional bit of resolution when approaching the KT/C noise limit, leads to 4x larger capacitance, with an equivalent increase of power consumption. Therefore, maintaining very low FOM with increasing ENOB is quite challenging and definitely not straightforward. Most comparator architectures stop working once the supply voltage reduces below approximately 750-800 mV. This research proposes an alternative approach to this challenge.
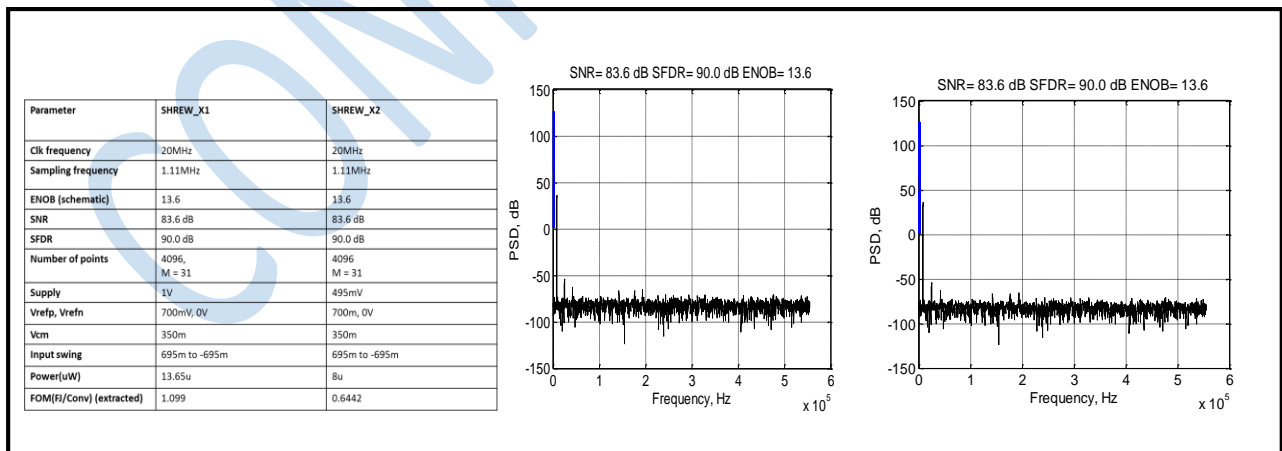
Target Specifications:

	Hsieh ISSCC 2018	Hsieh JSSC 2016	Tai ISSCC 2013	Harpe ISSCC 2014	Harpe ISSCC 2008	Harpe ISSCC 2015	Harpe ISSCC 2013	This work
TECHNOLOGY	90nm	90nm	40nm	65nm	65nm	65nm	65nm	65nm
SUPPLY	0.4	0.3	0.45	0.8	1	0.6	0.6	1, 0.5
SAMPLE RATE(S/s)	250K	600	200	32	1M	100	40	1M
RESOLUTION	13	11	10	14	10	10	10	14
POWER(nW)	638	187	84	352	1900	88	72	13u, 8u
ENOB	11.93	9.46	8.95	11.29	8.95	9.2	9.4	12.2
FOM(fJ/con)	0.6	0.44	0.85	4.4	0.85	1.5	2.47	1.8,1.1

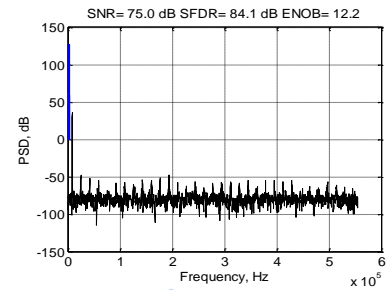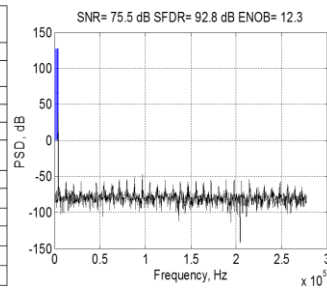## ADC Architecture and Model: (shrew x1 and x2)
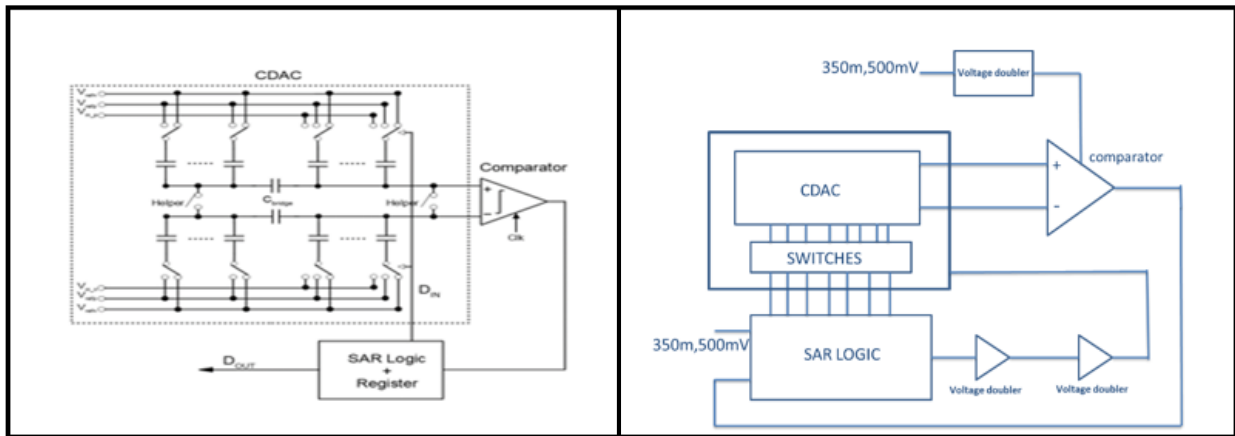
 We taped out two architectures. The regular split CDAC array architecture (Shrew X1) is designed with each of the blocks to get maximum performance for the power metric at 1V. In the second version (Shrew X2), with a reduced supply voltage of 500mv, we are boosting the power supply to the optimum operating voltage of each of the blocks rather than designing the blocks to a lesser supply voltage.

TL schematic Simulation Results:

Parameter	SHREW_X1	SHREW_X2
Clk frequency	20MHz	20MHz
Sampling frequency	1.11MHz	1.11MHz
ENOB (schematic)	13.6	13.6
SNR	83.6 dB	83.6 dB
SFDR	90.0 dB	90.0 dB
Number of points	4096, M = 31	4096 M = 31
Supply	1V	495mV
Vrefp, Vrefn	700mV, 0V	700m, 0V
Vcm	350m	350m
Input swing	695m to -695m	695m to -695m
Power(uW)	13.65u	8u
FOM(FJ/Conv) (extracted)	1.099	0.6442

SNR= 83.6 dB SFDR= 90.0 dB ENOB= 13.6

SNR= 83.6 dB SFDR= 90.0 dB ENOB= 13.6

Transient noise results:

Parameter	SHREW_X1	SHREW_X2
Clk frequency	20MHz	20MHz
Sampling frequency	1.11MHz	1.11MHz
ENOB (schematic)	12.3	12.2
SNR	75.5 dB	75 dB
SFDR	92.8 dB	84.1 dB
Number of points	4096, M = 31	4096 M = 31
Supply	1V	495mV
Vrefp, Vrefn	700mV, 0V	700m, 0V
Vcm	350m	350m
Input swing	695m to -695m	695m to -695m
Power(uW)	13.65u	8u
FOM(FJ/Conv) (extracted)	1.9	1.1

SNR= 75.5 dB SFDR= 92.8 dB ENOB= 12.3

SNR= 75.0 dB SFDR= 84.1 dB ENOB= 12.2

Future work:

- SAR logic for version 1 needs to be replaced with high Vt transistors to mitigate the leakage current.
- Need to increase the input signal range to get better ENOB rather than increasing the unit capacitance.
- 350m volt ADC with the use of Tripler.
- Remove bridge capacitance.