

ANNUAL REPORT 2019



MCCI
Microelectronic Circuits Centre Ireland

**TECHNOLOGY
CENTRE**
ENTERPRISE IRELAND
IDA IRELAND SUPPORTED





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CHAIRMAN AND EXECUTIVE DIRECTOR'S MESSAGE

CHAIRMAN'S MESSAGE

The Microelectronic Circuits Centre Ireland (MCCI) has a unique relationship with Tyndall National Institute, Enterprise Ireland and IDA. The on-going collaboration and specialist ecosystem that has been developed allows a team of world-class researchers and postgraduate students to deliver excellent application driven research. This has contributed to positioning Ireland as a global location for microelectronics companies, thereby contributing hugely to the vibrant microelectronics industry.

The Irish Government, through Enterprise Ireland and IDA, are investing significant funding and resources into the centre. It is recognised that MCCI gives existing indigenous companies a large competitive advantage as well as helping in the creation of new start-up companies. The end result being an increase to indigenous employment and export revenue. MCCI has become the de-facto conduit for IDA clients entering the Irish microelectronics system, and we are very encouraged by the number of semiconductor companies establishing or expanding their circuit design R&D operations in Ireland.

One of the key success of the centre is how it has become a source of talented and experienced researchers for industry, know-how and industry relevant IP, which give a competitive advantage to our members leading on to increased revenue, profit and employment. This is evidenced in the researcher profiles and IP that are featured in this year's report, these are the future leaders who will bring the sector to the next level in terms of employment and contribution to GDP. MCCI member companies employ almost 13,000 people in high value jobs, a 14% growth in employment from 2018. There is also a strong indigenous sector which has in the past number of years has seen VC investments of over €184M and exits over €100M.



MCCI has become the go-to place for industry to carry out research with academia for microelectronics, and will continue to focus on microelectronics circuits servicing the €9B export industry in Ireland. It is no coincidence that some member companies have strengthened their R&D presence in Ireland as a result of collaborating with MCCI, which is a huge achievement. The centre has ambitious plans in place to scale, which will undoubtedly lead to further enhancing Ireland as a leading country for attracting foreign direct investment and new microelectronics start-ups.

Donal Sullivan
Chairman

EXECUTIVE DIRECTOR'S MESSAGE

As a centre, we are well established as a single point of contact for access to high calibre experts in the field of microelectronics. Hosted in Tyndall National Institute, our team consists of almost ninety researchers and engineers across six research institutions, collaborating on over fifty projects. The team profiles featured in this report are testimony to the calibre of talent in MCCI. The report aims to showcase the scope and depth of the research we are engaged in. The changes year on year demonstrate the pipeline of talent that has transferred to Irish industry. Central to our success is our people who consistently work to deliver world class research outcomes.

Over the next five years we will continue to grow and scale the centre, to realise our vision to be a world leading Microelectronic circuit's research centre. I am pleased to report that after extensive consultation and engagement with our members in 2019, we have submitted a funding proposal to Enterprise Ireland for the next phase of MCCI. Negotiations are at the final stages and I anticipate sharing the positive outcome very shortly.

Microelectronic circuits are a key enabling technology, which are fundamental to, and underpin all electronic systems, and this research is central to the advancement of this sector. Despite 2019 being a down year for semiconductors, by the end of 2019 we are seeing a recovery begin as the global industry sees strong growth return, driven by changing technology cycles and market drivers. At the time of writing the Coronavirus pandemic is unfolding, and having a dramatic impact not just on our sector but across the world. As a centre we have adapted exceptionally well, completing a number of tapeout during that transition. This resilience is characteristics of the centre and the attitude of our people. As the impact of Coronavirus is fully realised in the coming year, we have a greater responsibility than ever to support our industry partners, as we get the whole sector moving again.

We are in a unique position to bridge the gap between industry and academia to move apace with industry growth. Two of the major industry growth drivers have been the proliferation of complex electronic devices especially in automotive and medtech applications, and the growing amount of semiconductor content per device. Electronic products are becoming more complex, and with a growing level of semiconductor content. Our growth plans are

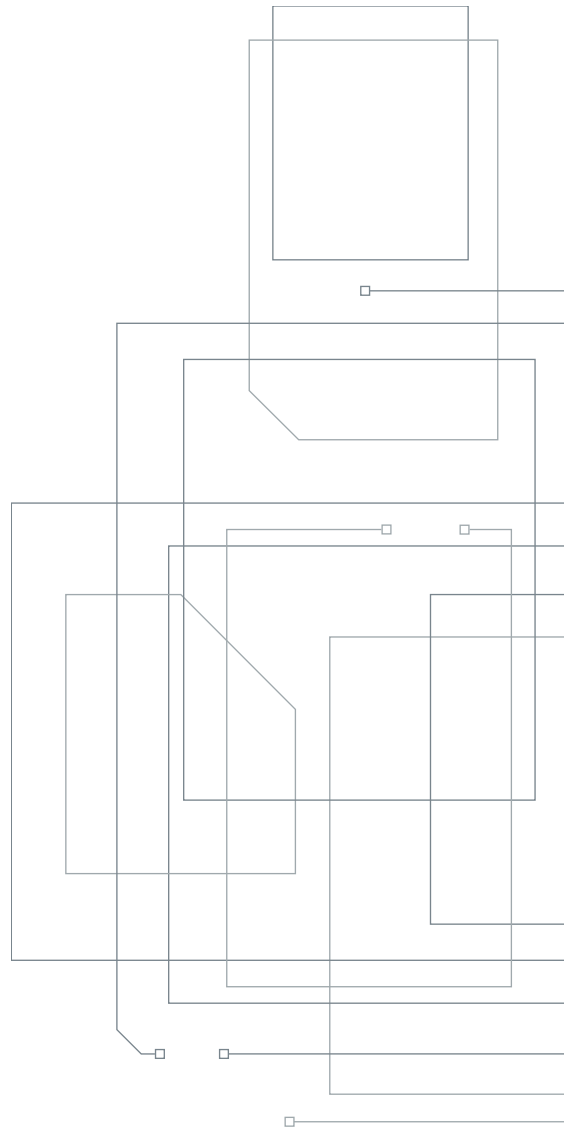


consistent with national strategies such as Innovation 2020, the National Development Plan 2018-2027 and Future Skills Needs 2017-2022 where we will continue to excel at meeting the critical needs of industry.

The content of this report showcases the level of expertise from our professors, principal investigators, senior researchers and students who consistently work on ground breaking circuit research. By providing our world-leading research, we provide competitive advantage to microelectronics companies (SMEs and MNCs) located in Ireland. Ultimately leading to increases in employment, export revenue and the generation of future leaders in the sector.

I would like to take this opportunity to thank our staff and students for their ongoing hard work and commitment as they work to make an impactful difference to the sector through their research. The continued growth and success of MCCI is due to their expertise and unique skillset to deliver innovative ground breaking research for industry.

Donnacha O'Riordan
Executive Director



ABOUT US

The Microelectronic Circuits Centre Ireland (MCCI) was founded to deliver high impact research for the semiconductor industry. Funded by Enterprise Ireland and the IDA, the role of MCCI is to generate innovative technologies. MCCI acts as a single point of contact for the microelectronics industry in Ireland to access academic research. The centre has an annual research revenue in excess of €8.1million and a team of over 90 researchers and engineers across Tyndall National Institute, UL and UCD, collaborating on more than 50 research projects.

MCCI undertakes collaborative projects in the microelectronics circuit design space with an emphasis on mixed-signal, Analogue and RF circuits. Projects may have algorithm, digital design, IC architecture or system architecture components to them where these can lead to improved performance of mixed-signal circuits.

VISION AND MISSION

To be the number one microelectronic circuits research centre globally, for industrial and academic collaboration by 2025.

To deliver high impact research outcomes, and by doing so develop our researchers into independent thinkers and future leaders in Irish companies and in the global semiconductor landscape.

RESEARCH PILLARS



High Speed
Transceivers



Power
Management



Precision
Circuits



Digital

APPLICATIONS



Future Networks
Communications
& IOT



Sustainable
Living



Medical
Devices



Diagnostics



Health &
Independent
Living



Smart Sustainable
Food Production
Processing

2019 HIGHLIGHTS

Feb 2019

Prof. Peter Kennedy, Scientific Director MCCI presented at ISSCC

Our Scientific Director, Professor Michael Peter Kennedy presented his paper on “4.48GHz 0.18 μ m SiGe BiCMOS Exact-Frequency Fractional-N Frequency Synthesizer with Spurious-Tone Suppression Yielding a -80dBc In-Band Fractional Spur “ at The International Solid – States Circuits Conference ISSCC.

May 2019

MTC – MCCI Technical Conference was held at the Engineering & Material Science Centre in University College Dublin.

MCCI’s Technical Conference is an annual event where we examine key microelectronic trends and novel academic papers. The event is a private event for our industry partners and research teams to gain insight and knowledge. There were four sessions on

- RF and PA Design
- Frequency Synthesis
- Data Converters
- Analog Circuit Techniques



The conference provides our members with access to novel information, key insights, and direct access to microelectronic research experts. The event is of very high value to our members as they will gain advance insight to our research breakthroughs.

September 2019

MCCI attend the National Ploughing Championships in Fenagh, Co. Carlow

Members of the team went to the National Ploughing Championships to showcase the first prototype of “Bovisense”, an on-farm diagnostic kit. The system is an innovative point-of-care bovine disease diagnostics system for vets, which diagnoses a range of IBR related viruses within 15 minutes. A multi-disciplinary team led by MCCI in collaboration with the Nanotechnology group from Tyndall National Institute are working to commercialise the product to bring it to market.

They won a Certificate of Achievement for being a finalist in the Innovation Arena.



November 2019

Engineers Ireland Awards

Matthew Agnew, Masters Student MCCI and Conor Healy, who was an Intern MCCI won prizes at the Engineers Ireland and Institution of Mechanical Engineers Awards 2019. They were awarded 2nd place in the Best Individual Applied Student Engineering Project competition. Matthew won in the postgraduate category while Conor won for the undergraduate category.



We host a range of webinars throughout the year to keep our industry partners up to date on the advances in our research.

Webinar Series	Speaker
Quantum Bits (Qubits) Implemented through Electrostatically Coupled Quantum Dots in Nanometer-Scale CMOS	Elena Blokhina
An Adaptive-Resolution Quasi-Level-Crossing-Sampling ADC Based on Residue Quantization in 28-nm CMOS	Hongying Wang
Intuitive Understanding of Flicker Noise Reduction via Narrowing of Conduction Angle in Voltage-Biased Oscillators	Yizhe Hu
A 31-W, 148-fs Step, 9-Bit Capacitor-DAC-Based Constant-Slope Digital-to-Time Converter in 28nm CMOS	Peng Chen
Challenges in On-Chip Antenna Design & Integration with RF Receiver Front-End Circuitry in Nanoscale CMOS for 5G Communication Systems	Mahsa Hedayati
Panther - a High Precision sub 1V ADC in 28nm CMOS	Daniel O'Hare
Passive Switched-Capacitor DS Modulator Based on Pipelined Charge-Sharing Rotation in 28-nm CMOS	Hongying Wang
A 0.2-V 30-MS/s 11b-ENOB Open-Loop VCO-Based ADC in 28-nm CMOS	Viet Nguyen

RESEARCH OVERVIEW

Our research roadmap is centred around the delivery of innovations for the broad range of applications listed below. Microelectronics is a key enabling technology for all these applications and our aim is for all of our research to be world beating.

Future Networks, Communications and IOT

- Beyond 5G cellular infrastructure for mobile phone technology.
- Satellite and mmWave communications.
- OptoElectronics and PICs.
- Ultra-low Power Radio.

Medical Devices & Technologies and Connected Health

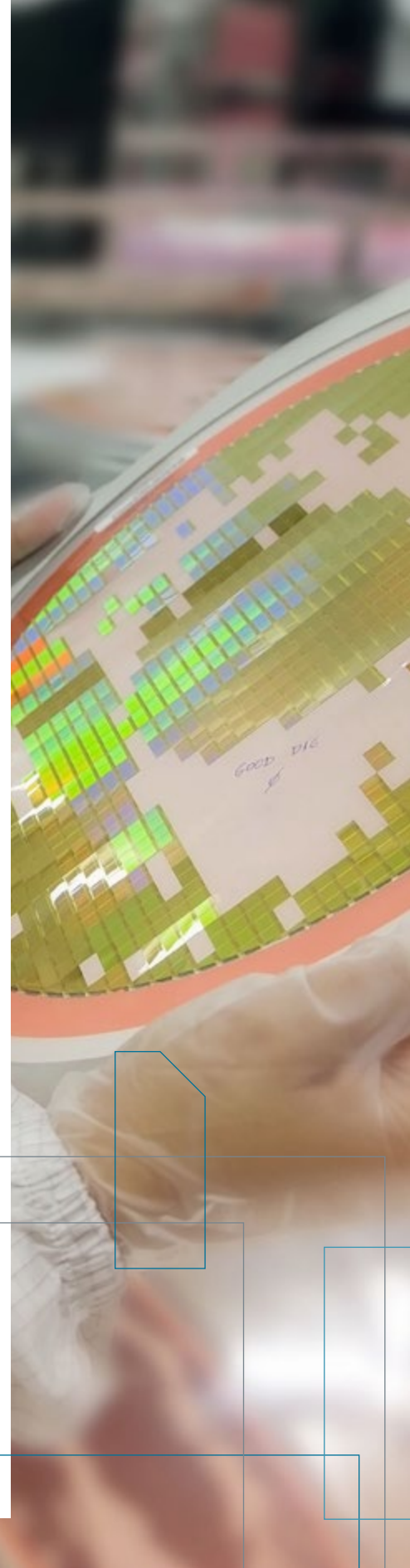
- RF sensing namely depth, distance and composition.
- Biosensing and neuromodulation.
- On-body wearable and in-body implantable.
- Point of care, imaging and robustness.

Smart Agri, Industrial and Automotive

- Smart Agri, and animal diagnostics.
- Sustainability and water quality.
- Green Energy - battery monitoring, health and charging.
- Machine monitoring and fault tolerance.
- Radar and antenna.

Digital and Processing

- Quantum and cryogenic.
- Artificial intelligence, machine learning and edge processing.
- Security and cryptographic technologies.
- Robotics navigation, sequencing engines and annealing processors.



HIGH SPEED TRANSCEIVERS

Our high-speed transceivers research pillar is focused on optical transceivers, mm-wave transceivers & systems, Hybrid RF Systems, and Hybrid GaN/CMOS/MEMs System-In-Package.

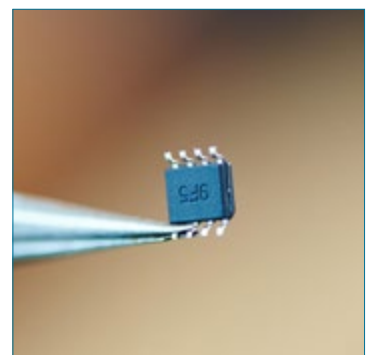
Our researchers are addressing the challenges that our industry partners need to enhance next-generation products. The increasing demand for broadband and 5G communications, with the use of massive multiple input and output (MIMO) and mm-wave technologies, drives demand for research in this space. The exponential growth of IoT, with sensing and imaging applications at sub-mm-wave frequencies being a key driver, allows us enhance performance and efficiency in these applications. Demand for faster wireless-data rates, within the context of mobile-battery limitations, drives the development of high-throughput and power-efficient transceivers.

An example of one of our collaborations enables a widespread deployment of devices and sensors utilizing existing cellular infrastructure. In this instance we are working on a beyond state-of-the-art solution in per bit efficiency for high data rate, low frequency transceivers.

Another ground-breaking project is the design of a high-performance chip for 5G applications

which aims to achieve higher resolution and lower power consumption. The objective is to enable cost reduction and enhanced battery life. The efficiency we can expect to obtain will be more than 35%. The benefits for end applications is the higher circuit integration level suitable for mobile devices, which delivers higher power efficiency and better battery performance.

In the bio-photonics research space, we deal with diffuse light within tissue. Light is absorbed and scattered depending on the wavelength and tissue properties. The deeper we image in tissue the smaller and more complex the optical signal becomes. Optical detectors are often pushed to the limits of detectability. The overall detection system is also heavily dependent on the interface electronics to the detector and its location. Optimisation demands new levels of integration requiring co-location of the TIA, wide dynamic range, AGC, and communications. The research challenge at this level of integration is achieving a beyond state-of-the-art optical detector interface circuit and system design, which will enable more sensitive measurement in tissue. If successful this will assist clinicians to image and measure critical medical parameters, improving the quality of patient care.

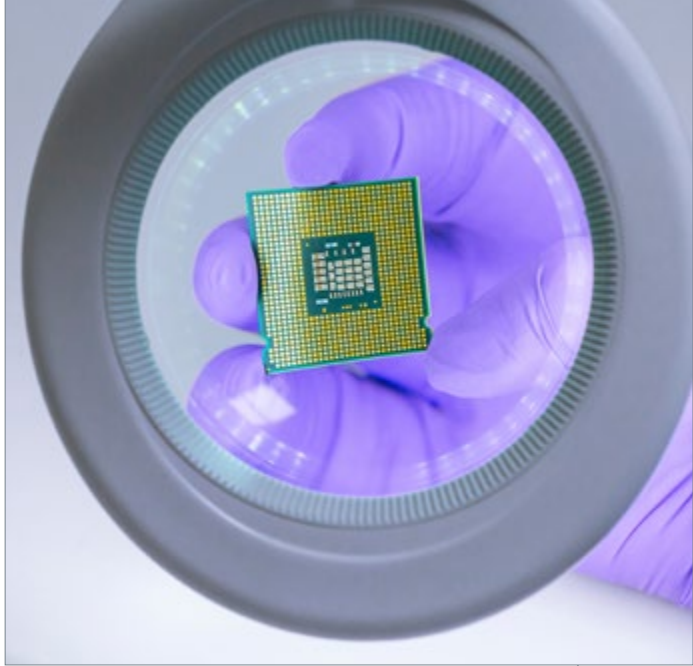


PRECISION CIRCUITS

Our precision circuits pillar is centred on the delivery of state-of-the-art data converters and analogue front ends. There is a specific focus on sensor interface circuits, targeting applications including Smart Agri and point-of-care diagnostics. We work on capacitive and resistive sensor interfaces and time-based converters. Key research challenges include increased precision, noise immunity, increased bandwidth and linearity, and power efficiency, as measured in energy per conversion step.

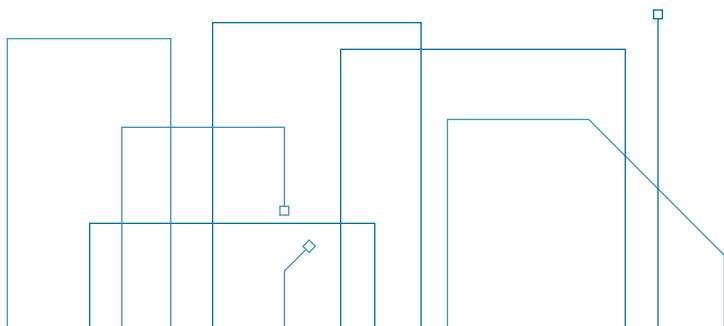
We are developing noise-shaped SAR ADCs in 28nm CMOS, which are implementing novel architecture and circuit techniques to increase precision and mitigate noise. We are also leveraging a host of new sensing methodologies that have emerged in electrochemistry and biological sensing over the past decade.

Noise-shaping techniques are shown to increase the resolution by two effective number of bits. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic all of which benefit from faster CMOS technologies. The objective of this is to leverage this speed advantage through oversampling and noise-shaping to achieve an ADC with greater precision. An important research driver in this space is improving on state-of-the-art in figure-of-merit and PPA (power performance area) of the circuits. We have already developed some of the best performing SAR ADCs from a power consumption point of view, with 10bits of resolution and a signal bandwidth of less than 1MHz. Future research aims to further



the state-of-the-art in high-sensitivity current measurements at >10MHz bandwidth. In this regime, high AFE noise in the presence of large sensor capacitance is the limiting factor. Hence the research aims to use circuit techniques to mitigate this high AFE noise which has traditionally limited similar current readout solutions.

We work on ultra-low power and sub-threshold voltage research projects. Further advancements in the state-of-the-art are necessary for future Biomedical, IoT and Smart Agri based applications. Such ADCs typically target sub 1kHz sampling rate and 12-16 bit resolution. Initial focus is on developing ADCs with a power consumption target of less than 1μW and a Schreier FoM of 180+ dB. Secondly we can target reducing the leakage current, reducing the start-up time that the circuits require, improving the duty cycle efficiency, and extending the resolution achieved.



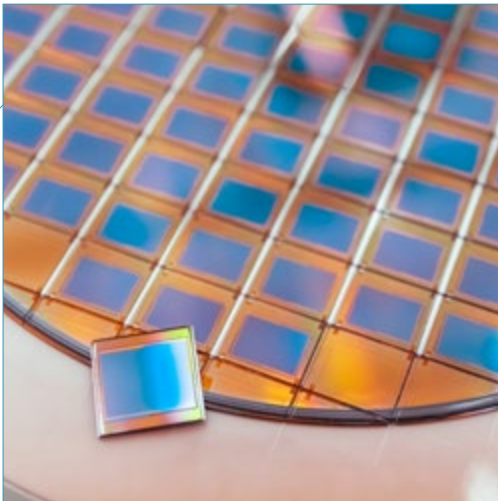
POWER MANAGEMENT

Our research focus in power management is on highly integrated conversion, for example reducing the size and the need for external discrete components, and on energy harvesting – managing the source and storage of multiple micropower sources.

We are looking at the emerging area of hybrid and resonant switched-capacitor topologies that deliver better utilization of active semiconductors and passive components. We are presently developing highly integrated conversion to improve electromagnetic interference, efficiency and reliability. Energy harvesting projects include the development of integrated voltage regulation and novel topologies.

One of our research projects is exploiting advanced integrated magnetics for mobile and portable device point-of-load (3-7V POL) conversion. The objective is the removal of large external discrete chip inductors, transitioning to a much more highly integrated power system-in-package or in-die.

The research goal is granular power, where the performance of mobile SoC voltage regulation (high dynamic performance 1.8V to Core & IO voltages) becomes much more highly integrated and segmented to multiple voltage domains, enabling a multi-fold increase in battery life, dynamic performance and across-die thermal gradients.



DIGITAL

Within IoT applications, as security moves from being an add-on algorithm to a hardware solution implemented at the circuit level, circuits for cyber security has emerged as a key enabler. Secure-by-design is the overarching research output where safety is critical in operation in industrial control, public welfare and other applications.

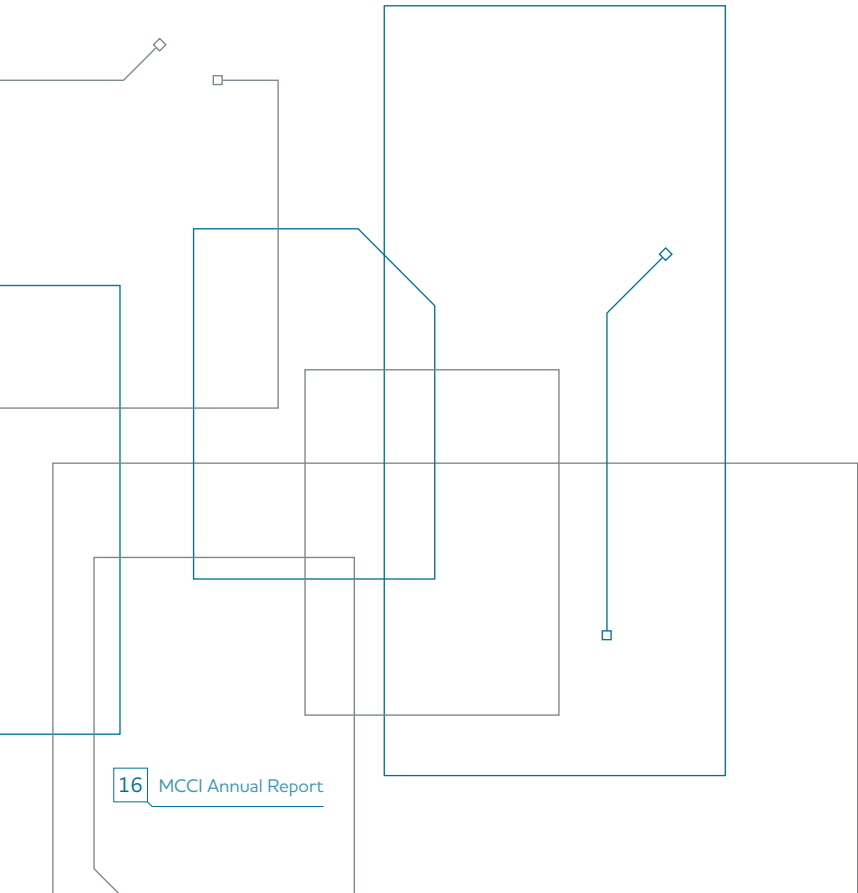
Crypto circuit implementation, true RNG and private data security, where AI training features are integrated at the edge device, are all current areas of research interest. Improving energy efficiency and higher throughput become even more important as we implement NPUs (Neural Processing Unit) on edge devices, where our key metrics are Energy per Inference and Inference per Sec.

Physically tamper proof and Intellectual Property (IP) protection against reverse engineering are two examples of current research in this space, as the industry is increasingly concerned with

the growing risk of supply chain contamination by counterfeit devices.

The scope of our research also extends to efficient architectures and implementation of arithmetic functions approximation-based stochastic computing, as alternatives to binary computing for a number of low-power embedded systems. We are also looking at exploiting technology features, such as body biasing and passive device advancements, as we work to improve PPA (power, performance, area) of digital circuits.

Quantum engineering is an emerging field we are committed to addressing, initially looking at cryogenic temperature circuits, and the behaviour of CMOS circuits at cryogenic temperatures. Research is underway to examine circuits to control and observe quantum devices, ultimately addressing quantum computing applications.



CURRENT MEMBERS



IP REGISTER

IP AVAILABLE FOR LICENSING

Description	Owning PRO	Research Lead
A 100dBfs SFDR Band-Pass $\Sigma\Delta$ Current-Steering DAC in UMC 90nm	UL	Brendan Mullane
0.32mm ² , 0-6GHz, 4ps rms Multi-band LC VCO PLL	NUIM	Ronan Farrell
A continuous time front end for ADC in 28nm SOI	UL	Tony Scanlan
0.35 μ m CMOS Instrumentation Amplifier	UCC	Ivan O'Connell
0.35 μ m CMOS nano-watt 32.768KHz always-on clock generator	UCC	Ivan O'Connell
0.35 μ m CMOS nano-watt 12b SAR ADC utilizing a 32KHz clock & converting at 800Hz	UCC	Ivan O'Connell
0.35 μ m CMOS nanowatt differential input & output bandpass filter	UCC	Ivan O'Connell
Digital Control from Innovation partnership	UL	Mark Halton
Digital Control synthesis tool from CFTD	UL	Mark Halton
0.35 μ m CMOS thoracic impedance circuit used to infer respiratory rate	UCC	Ivan O'Connell
0.35 μ m CMOS nanowatt voltage reference & bias current circuit. Vref is independent of temperature & power supply variation	UCC	Ivan O'Connell
0.35 μ m CMOS low power PMIC that uses an external inductor to increase a Vin (varying from 2V to 3V) to a higher Vout, programmable up to 18V.	UCC	Ivan O'Connell
0.35 μ m CMOS Pacing Block which charges a Pace Capacitor via a current source. The Pace Capacitor is discharged in a controlled manner to force the heart to beat.	UCC	Ivan O'Connell
0.35 μ m CMOS Neurostimulation pulse generator can operate up to 18 Volts, and delivers biphasic currents	UCC	Ivan O'Connell
0.35 μ m CMOS Digital Block for controlling Pacing or Neurostimulation	UCC	Ivan O'Connell

IP AVAILABLE FOR LICENSING

Owning RPO	Research Lead	Category	IP Block	Description	Status
UCC	Peter Ossieur	PAM-4 CDR	Components for analog phase locked loop	STM 65nm CMOS, Phase detector, charge pump, analog filter, high-speed digital divider circuit with few programmable divider settings	Silicon Proven
UCD	Anding Zhu	ADC	Algorithm	Volterra-based RLS (Recursive Least-Square) algorithms for Digital Post-Correction of ADCs	
UCD	Anding Zhu	ADC	Algorithm	Algorithms for Non-uniform Analog Interpolated Multichannel Digital Post-Correction for Time-Interleaved ADCs	
UCC	John Doyle	AMS	Current Sense	0.35µm CMOS High-side Current Sensor	Silicon Proven
UCC	Kevin McCarthy	Power Management	DCDC	30MHz DC-DC Converter with Integrated Magnetics	Silicon Proven
UL	Tony Scanlan	ADC	ADC	65nm HiCOSANT SAR ADC with Novel Calibration	Silicon Proven
UCC	Peter Kennedy	PLL	Freq Div	Divide-by-three Injection-Locked Frequency Divider	
UCC	Ivan O'Connell	RF	Voltage Controlled Oscillator	High-performance Voltage Controlled Oscillators in a SiGe BiCMOS technology	Silicon Proven
UCC	Ivan O'Connell	RF	Varactor	High Q Varactor for High-performance Voltage Controlled Oscillators in a SiGe BiCMOS technology	Silicon Proven
UCC	Ivan O'Connell	ADC	Thermal noise reduction	Reduction of Sampled KT/C Thermal Noise for ADC	Simulation
UCC	Ivan O'Connell	AMS	TIA	3.3V 0.35µm transimpedance amplifier	GDS
UCC	Ivan O'Connell	AMS	Active Quench Circuit	Active quench circuit for use with Single Photon Avalanche Diode	GDS
UCC	Ivan O'Connell	AMS	Bandgap	3.3V supply 0.35µm 1.2V Bandgap Reference circuit	GDS
UCC	Ivan O'Connell	Digital	Ring Oscillator	0.35µm 666MHz ring oscillator with divide-by-32	GDS

Owning RPO	Research Lead	Category	IP Block	Description	Status
UCC	Ivan O'Connell	AMS	SPAD readout	0.35µm single photon avalanche diode pixel read out circuit	GDS
UCC	Ivan O'Connell	AMS	TDC	0.35µm time-to-digital converter	GDS
UCC	Ivan O'Connell	Digital	Standard-cells	0.35µm digital standard cells	Layout
UCC	Ivan O'Connell	Biomedical	Pace controller circuit	0.35µm CMOS low power Cardiac Pace Controller which interfaces with sense channels & microprocessor to handle multi-mode pacing	Silicon Proven
UCC	Ivan O'Connell	Clocking	Clock generator	0.35µm CMOS low power clock oscillator that generates a freq stable across power supply range, with adjustable pulse width	Silicon Proven
UCC	Ivan O'Connell	Biomedical	Chip	0.35µm CMOS low power chip that includes Atrium Sense, Ventricle Sense, Thorasic Impedance Sense, Atrium Pace, Ventricle Pace, Neurostimulation, Hysteric Boost Block and Real time Clock to enable Rate Responsive heart pacing	Silicon Proven
UCC	Ivan O'Connell	Biomedical	Chip	0.35µm CMOS low power chip that includes Atrium Sense, Ventricle Sense, Atrium Pace, Ventricle Pace, Neurostimulation, Hysteric Boost, Real time Clock and Pace Controller to enable heart sensing and pacing without the intervention of a micro controller	Silicon Proven
UCC	Ivan O'Connell	ADC	Capacitive-to-Digital converter	0.35µm CMOS Oversampled Sigma Delta ADC with extended Input Range	Silicon Proven
UCC	Ivan O'Connell	Digital	Asynchronous I2C Slave Interface	Asynchronous I2C Slave Interface	Silicon Proven
UCC	Ivan O'Connell	Sensor	Layout	Several permutations of Interdigitated Sensor Structure Test Chip	Silicon Proven
UCC	Ivan O'Connell	ADC	Sigma Delta Modulator	Sigma Delta Modulator on XFAB 0.35µm	GDS

Owning RPO	Research Lead	Category	IP Block	Description	Status
UCC	Ivan O'Connell	Biomedical	DNA Sensor Chip	0.35µm CMOS DNA Sensor Chip containing a high-resolution sigma-delta Capacitive-to-Digital converter, I2C Interface, bandgap reference, bias generator, 1MHz oscillator, Power-on-Reset circuits, EEPROM memory for ID coding, chip tracking, and sensor calibration coefficients.	Silicon Proven
UCC	Ivan O'Connell	ADC	SAR ADC Chip	28nm 13 ENOB noise-shaped SAR ADC	Silicon Proven
UCC	Ivan O'Connell	ADC	SAR ADC Chip	28nm 15 ENOB noise-shaped SAR ADC	GDS
UCC	Mark Smyth	Clocking	ADPLL	28nm 16GHz Low Power All-Digital Phase Locked Loop (DPLL)	Silicon Proven
UCC	Ivan O'Connell	ADC	SAR ADC Chip	65nm Low Power 1MS/s 12-bit SAR ADC, 76db SFDR, 62db SNR	Silicon Proven
UCC	Ivan O'Connell	ADC	SAR ADC Chip	130nm 2-MS/s 12-bit Extended Input Range SAR ADC with Improved DNL & Offset Calculation	Silicon Proven
UCC	Ivan O'Connell	ADC	High-speed ADC	28nm 1GS/s 8-Bit ADC	Layout
UCC	Bogdan Staszewski	RF	RF-DAC	28nm iDTX - an Interpolative Digital Transmitter with Quantization Noise and Replicas Rejection	Silicon Proven

RESEARCHER PROFILES

OUR RESEARCH LEADERS



Dr. Ivan O'Connell



Prof. Peter Kennedy



Prof. Bogdan Staszewski



Prof. Anding Zhu



Dr. Teerachot Siriburanon



Dr. Elena Blokhina



Dr. Deepu John



Mr. Seamus O'Driscoll



Dr. Padraig Cantillon Murphy



Dr. Barry Cardiff



Dr. Brendan Mullane



Dr. Darren Francis Kavanagh



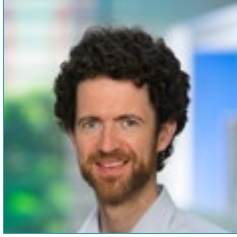
Dr. Emanuel Popovici



Dr. Ivan O'Connell, Head of Precision Circuits

Ivan joined MCCI in 2013 and is the Head of Group of the MCCI core research team. Since joining MCCI he has grown the MCCI core team to 20 researchers, which consists of Masters and PhD students, Postdocs, Research Assistants and Senior Researchers. His primary research interests are in the area of Analogue Mixed Signal Circuits and data converters. He is particularly interested in the application of this research in areas including: Internet of Things, Biomedical, Smart Agri and Energy Harvesting. He is currently a principal investigator in a number of Innovation Partnerships and Commercialisation Funds. He is involved in a number of H2020 projects. In addition, he is an SFI CONNECT Funded Investigator and is actively involved in the newly

funded SFI centre VistaMilk. Prior to joining MCCI, Ivan was the Design Manager in ChipSensors, which was subsequently acquired by Silicon Laboratories in 2010. While there, he lead the development of their digital relative humidity and temperature sensor products, from initial concepts, through to initial and interim prototypes, to their subsequent commercialisation, including custom test development. Since joining MCCI, he has secured €6 million in funding, in addition to 10 commercial licenses and transferring 27 trained researchers to industry. Since 2016, he is a member of the Custom Integrated Circuits Conference Technical Programme Committee.

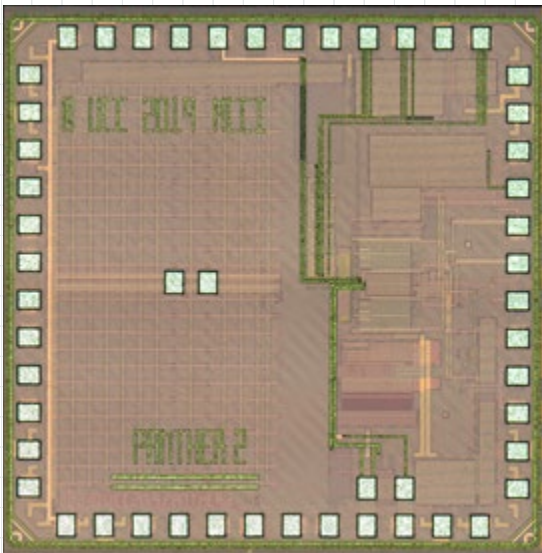


Dr. Daniel O'Hare, Senior Researcher

Daniel O'Hare received the BE degree in Electronic Engineering from University College Dublin in 2000 and completed his PhD at the University of Limerick in 2017. He joined Motorola Semiconductor 2000 and from 2004 to 2008 he was with Freescale Semiconductor designing ADCs and DACs for Cellular transceivers. From 2008 to 2012 he was Analogue Design lead with M4S NV a spinout of IMEC and from 2013 to 2017 he was an ADC researcher in the Circuits and Systems group at the University of Limerick. Since 2017 he is a Senior Researcher in MCCI based at the Tyndall National Institute. He lectures 'Advanced Analog IC Design' to UCC masters in Electronic Engineering students.

Current research: Danny's present research is in precision ADCs and low-noise sensor interface circuits. He is design lead/architect of the MCCI precision Noise shaped SAR project. He is also supervising Postgraduate research projects investigating precision current interfaces capable of detecting currents with pico-ampère precision. He has several on-going projects with the Bio-photonics group at Tyndall National Institute.

Research Topics: Danny's research interests are low noise, area and voltage analogue interface circuits and ADCs. These interests are applied in Sensor interface ICs with precision current sensing interfaces a strong interest.



A die photo of our Noise shaped SAR ADC targeting 15ENOB with a 0.9V supply designed in 28nm CMOS



Anita Schuler, Senior Digital Design Engineer

Current Research: 1.5GHz Noise-shaped SAR ADC on TSMC 28nm

Implementation of an ADC Non-Linearity Calibration Algorithm in the Xilinx Zynq UltraSca

Research Topics: Digital design for ADCs, including specification, design, Verilog RTL Coding, verification, synthesis, place and route and gate-level back-annotated simulations.

Digital PLL on TSMC 28nm

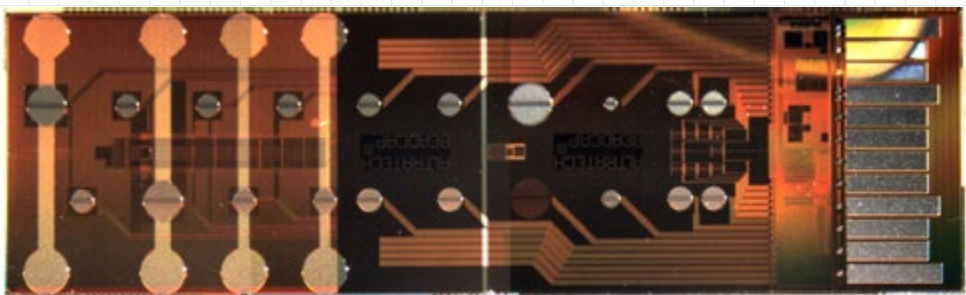
Digital-on-Top auto-routing using Cadence Innovus

Verilog and Digital Design consulting to other groups in Tyndall/UCD

Education: Anita holds a B. Eng (Electronic Engineering), University of Limerick, 1994. First Class Honours.

Work Experience: Anita previously worked as a Digital Design Engineer in Silicon and Software Systems (S3) in Dublin. She then moved to Galway and worked as a Senior Digital Design Engineer for Toucan Technology, which was later acquired by PMC-Sierra.

She also worked as an FPGA Design Lead for a start-up company called PortoMedia.



Top level die photo of a Capacitive to Digital Converter for Magnetic Bead detection in 0.35um CMOS process



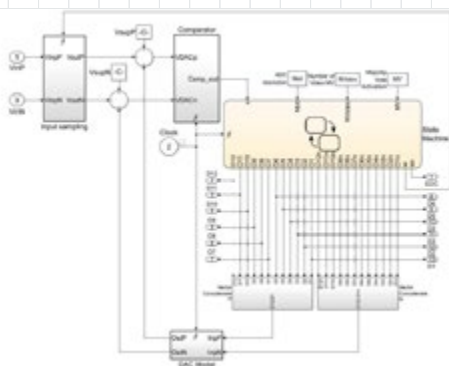
Dr. Gerardo Salgado, Senior Researcher

Current research: He is developing novel high resolution Analog-to-Digital Converter (ADC) architectures using digital signal processing techniques to compensate for analog circuit imperfections. He is also continuously developing/improving his Matlab(R)-based SAR ADC design toolbox, SIMSAR, which provides accurate simulation results at a highly reduced computational time. The SIMSAR toolbox is available to download free from charge at <https://www.mcci.ie/simsar-toolbox/>. (This toolbox has been already downloaded over 100 times from different universities around the world.)

Research topics: Design and implementation of SAR ADCs, Delta-Sigma Modulators (Digital,

Discrete-time and Continuous-time), Digital Signal Processing (Filter design), Machine-Learning assisted calibration and simulation algorithms for ADCs, Behavioural modelling, and Computer-Aided-Design tools.

Education: Gerardo Salgado received the B.S., M.S and Ph.D. degrees in Electronics Engineering from Institutes ITP and INAOE, Mexico, in 2009, 2011 and 2015, respectively. During his Ph.D. studies, he joined the Microelectronics Institute of Seville (IMSE), Seville, Spain, and Texas A&M University, USA, as a visiting scholar. Since January 2016 he has been working as a postdoc researcher at MCCI.



SIMSAR model and user interface



Aidan Murphy, PhD Student

Current Research: As sensing technologies develop, there is an increase in the demand to take measurements at the point of sample. MCCI are collaborating with the Nanotechnology Group in Tyndall to enable point of care electrochemical sensor detection. A variety of voltammetric techniques have been enabled on the data acquisition system. Results have been accepted for publication at the International Instrumentation and Measurement Conference, Houston, 2018 and IEEE Nano, Cork, 2018. The system is now battery powered and wireless connectivity has been enabled via Bluetooth. It can be interfaced to via an android smartphone application.

Current work is focused on enabling more electrochemical tests and miniaturising the system.

Current research is focused on implementing portable impedemetric biosensing on nano electrochemical sensors.

Research Topics:

- Embedded Systems
- Electrochemistry
- Nanotechnology

Education: Aidan received his BE degree in Electrical and Electronic Engineering from University College Cork in 2016 and is currently pursuing a PhD degree with MCCI, University College Cork

Electrochemical interface prototype for on farm disease diagnostics





Subhash Chevella, Senior Design Engineer

Current research: Current research involved in investigating the novel design ideas to improve the linearity and the noise for high precision analogue circuits. In addition, digitally assisted techniques to improve the performance of analogue engineering blocks.

Research topics: Low power techniques in deep-submicron technology

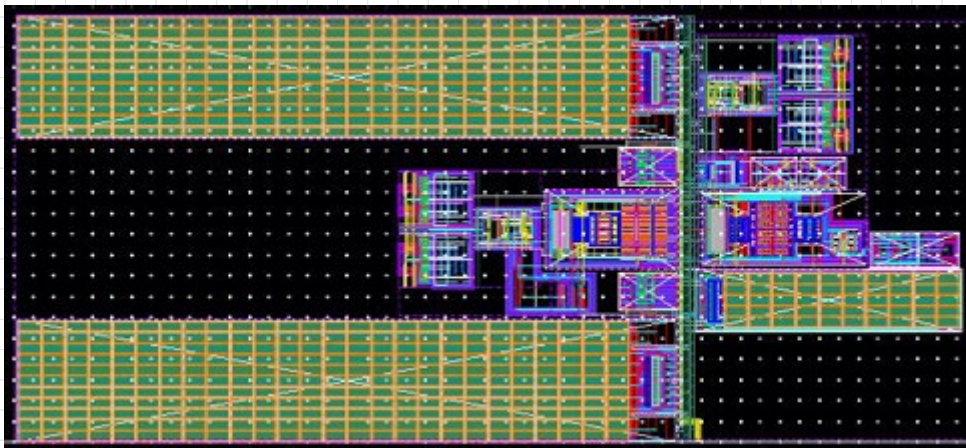
High speed, Low noise Dynamic amplifiers

High precision & Hybrid ADCs

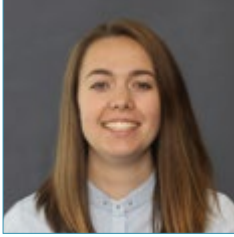
Education: Subhash Chevella is a PhD researcher at MCCI. The Primary focus of his research is precision analogue engineering blocks.

He completed his Master's in 2011 from DA-IICT, India. His Masters research was involved in Analysis of Charge injection, Clock feed-through and Capacitor mismatch in Switched Capacitor Circuits.

He completed his Bachelor's in Electronics and Communication in 2009 from JNTU, Hyderabad, India.



Low Noise Dynamic amplifier



Annamaria Fordymacka, PhD Student

Current Research: Temperature sensors are required in a vast number of applications such as food monitoring or MEMS compensation. Traditionally, the temperature sensor read-out circuitry would consist of a Wheatstone bridge followed by an instrumentation amplifier that would require high input impedance and low input-referred noise. While the design of such an amplifier is challenging, the design of the subsequent analog-to-digital converter (ADC) is equally if not more demanding, to ensure that these blocks do not limit the resultant achievable resolution and accuracy. There have been many attempts to remove the requirement for the input instrumentation amplifiers from temperature-to-digital converters, but the majority of these are based on either sigma-delta or VCO based ADC, which trade area for power. The research

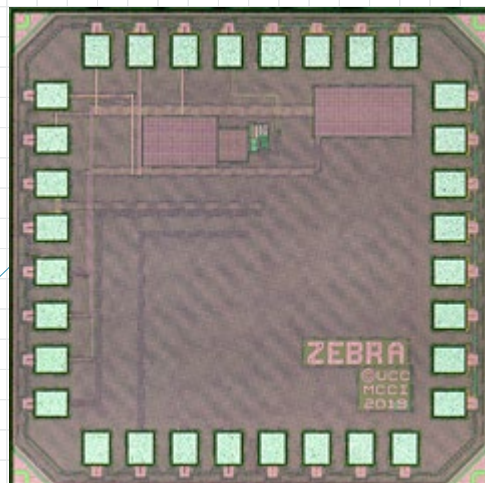
here is on designing a more efficient architecture for a bridge-to-digital converter.

Research Topics:

- Analog and Mixed-Signal IC Design
- Hybrid Data Converters
- Low Energy Applications
- Sensor Interfaces

Education: Annamaria graduated from UCC with a Bachelor's Degree in Electrical & Electronic Engineering in 2014. After her graduation, she joined MCCI at Tyndall National Institute where she completed her Master's degree in 2016. She is currently a PhD researcher in MCCI under the supervision of Dr Ivan O'Connell. The primary focus of her research is mixed signal/analogue IC design.

Die photograph of a Bridge to Digital Converter in TSMC 65nm

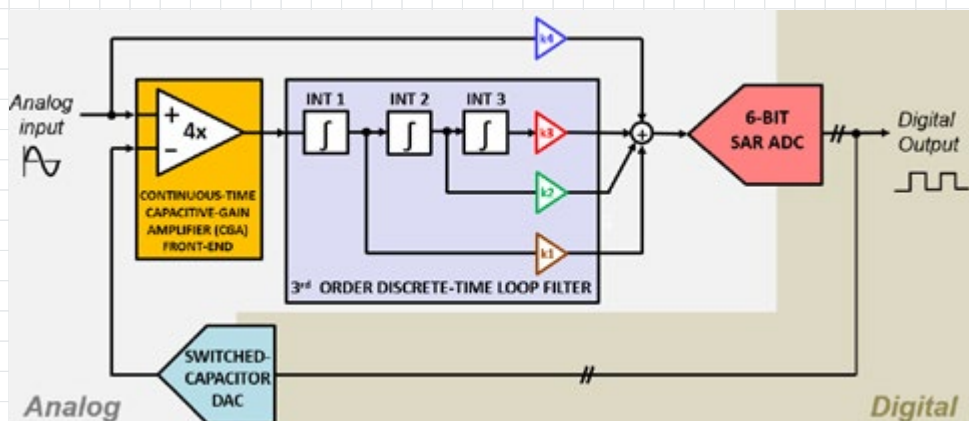




Spyros Kalogiros, PhD Student

Spyridon (Spyros) is currently a Ph.D. Student / Researcher and a member of Microelectronic Circuits Centre Ireland (MCCI), part of Tyndall National Institute in Cork, Ireland. He received his B.E. degrees in Electronic Engineering Education and in Electronic Engineering, in 2010 and 2011 respectively, both from the School of Pedagogical and Technological Education in Athens, Greece, and his M.S. degree in Electronic Physics / Radioelectrology from the Physics Department of Aristotle University of Thessaloniki, Greece, in 2015. He has held internship positions with COSMOTE S.A. in Athens, Greece, as a broadband network engineering trainee

for the operation, maintenance and upgrade of its 3G mobile network, and with MCCI, where he has worked on an implantable and fully integrated biopotential acquisition chip, for cardiac pacing and sensing purposes. His current Ph.D. research is on the field of Delta-Sigma Analog-to-Digital Converters, aiming to develop new design guidelines and solutions for higher performance in terms of higher Figure-of-Merit, and therefore, to set higher state-of-the-art specifications, as imposed by the ongoing and increasing demand for even more efficient Analog-to-Digital Converters over the next few years.



A 6-bit 3rd order High Performance Delta-Sigma Modulator with a Continuous-Time Capacitive Amplifier Front-End

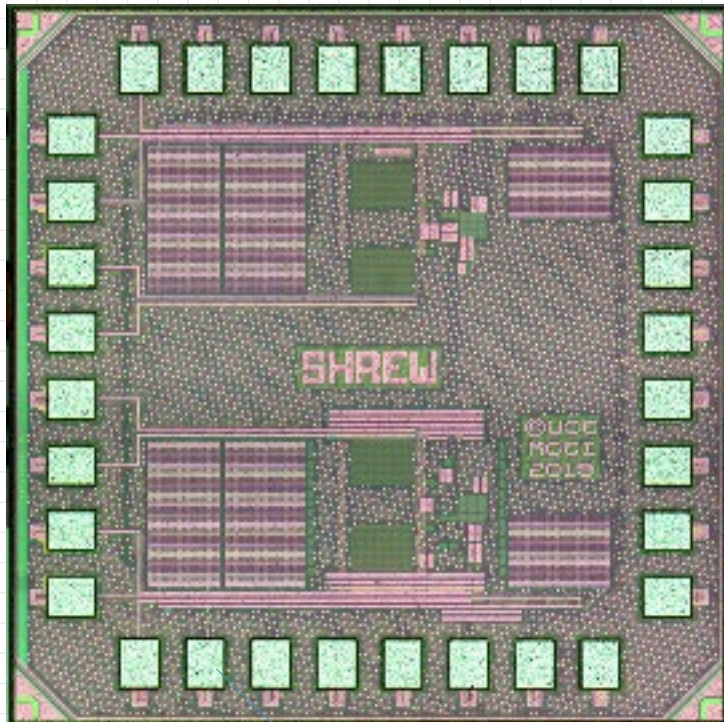


Madhan Venkatesh, PhD Student

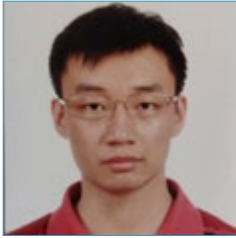
Current research : Developing low power and low voltage analog to digital converters on TSMC 65nm.

Research topics: low voltage and low noise comparator design, low power digital circuits, sampling circuits breaking the KT/C thermal noise Limit, SAR ADC'S.

Education : B.E. in electronics and communication from Visvesvaraya Technological University, Karnataka, India and is currently pursuing the PhD degree with MCCI, University College Cork



Die micrograph of 1V and 500mV 14 bit SAR ADC.



Hao Zheng, Research Assistant

Current research: Implementation of high-resolution data converter in 28nm CMOS processes for IoT application.

Building DPLL and noise model for the clock jitter research, based on Matlab and Simulink.

Analysis and research jitter suppression techniques for the high-resolution converter.

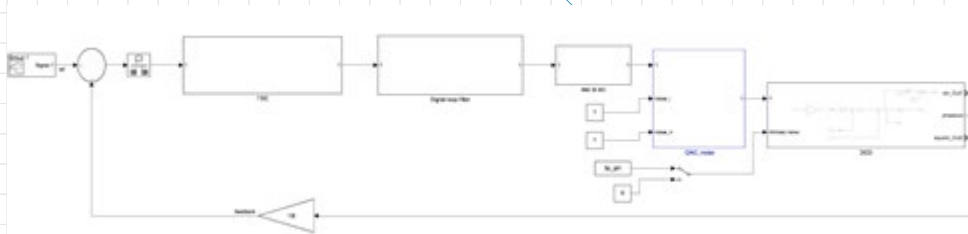
Research Topic:

- CMOS Analog IC design, Mixed-signal system modelling and design.
- DPLL & its noise modelling

Education: Master of Engineering Science, University College Dublin, Dublin, Ireland(2017)

Bachelor of Engineering, Lanzhou University of Technology, Lanzhou, Gansu, China(2013)

Digital phase locked loops model in Simulink





Anthony Wall, PhD Student

Current Research: A host of new sensing methodologies have emerged in electrochemistry and biological sensing over the past decade. The physics of many of these sensing topologies require charge-based rather than potential-based measurement. Thus there is a requirement for high resolution current-to-digital readout solutions, often in arrays. Anthony is researching the wide-bandwidth acquisition and digitization of current signals using novel Analog-to-Digital conversion methods. Wide bandwidth current readout presents a host of challenges in terms of noise, bandwidth and power consumption. Anthony intends to exploit novel circuit architectures, such as the Flipped Voltage Follower Current Conveyor, to improve the state of the art in wideband Current-to-Digital conversion. MIDAS 3rd Level Project of the Year Winner for 'Design and Stimulation of an Analog Front End for Cancer Detection by

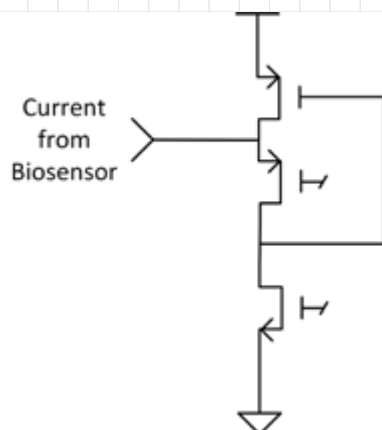
Fluorescence Imaging 'UCC School of Engineering Joe Gantly Prize Winner for design of Sigma-Delta Converter while on placement with Cypress Semiconductor

Research Topics:

- Current-Mode Sensor Interfaces
- High-Resolution Current Measurement
- Wide Bandwidth TIA Frontends
- Nanoscale Sensor Modelling
- Current-Mode ADC design
- Nanopore-based DNA Sequencing

Education: Anthony graduated from University College Cork with 1st Class Honors in the BE degree in Electrical & Electronic Engineering in 2018, and is currently pursuing the PhD degree with MCCI, University College Cork in the area of Mixed Signal Circuit Design.

Transimpedance Amplifier Alternatives - The Improved Common Gate Circuit





Michael Pastoril, Senior IC Layout Engineer

Education: Bachelor of Science in Electronics and Communications Engineering Polytechnic University of the Philippines Manila 1998.

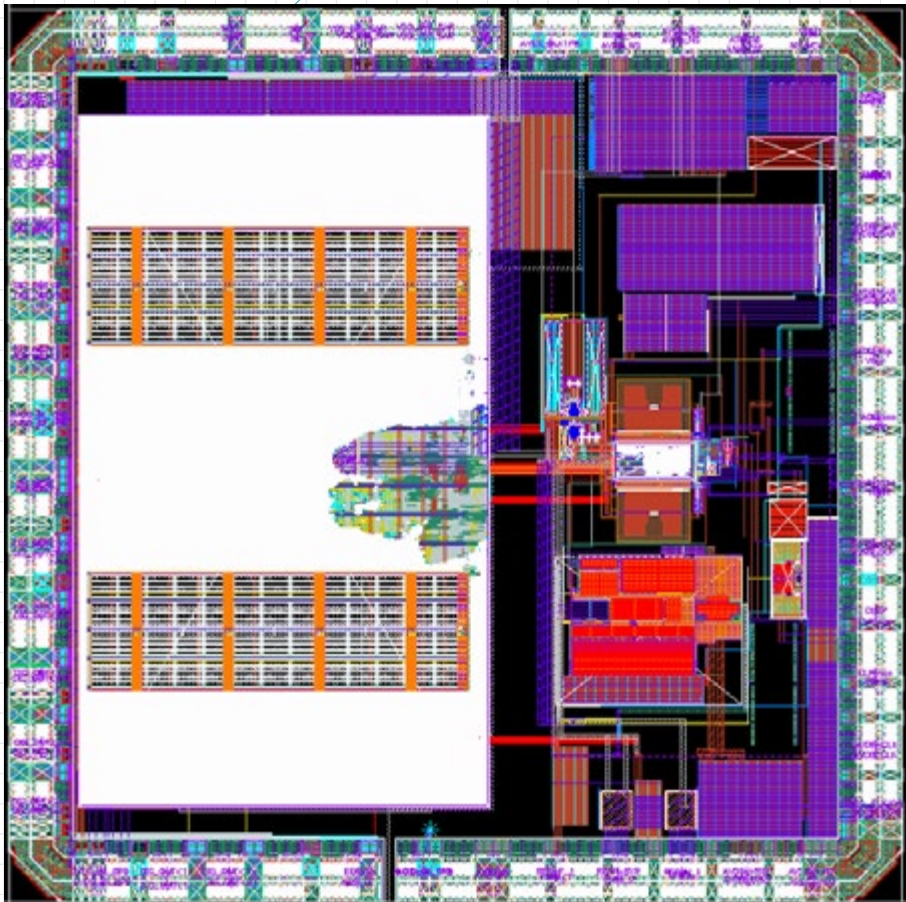
Current Project research: 1.5GHz / 16Bit Noise Shaped SAR ADC on TSMC 28nm

14Bit SAR ADC on TSMC 65nm

DC-DC Converter with Inductor Integration on TSMC 28nm

Research Topics: High-Speed Transceivers, High-Precision Circuit and Power Management.

Noise shaped SAR ADC 16 bit ENOB at 1MSPS





Prof. Peter Kennedy

He received his BE (Electronics) degree from UCD in 1984, his MS and PhD from the University of California at Berkeley in 1987 and 1991, respectively, and the DEng from the National University of Ireland in 2010. He joined UCC as Chair of the Department of Microelectronic Engineering in 2000. He served as Dean of the Faculty of Engineering from 2003 through 2005 and as UCC's Vice-President for Research from 2005 to 2011. He moved to UCD in 2017. He has over 400 research publications (including four patents) in the fields of oscillator design, hysteresis, neural networks, nonlinear dynamics, chaos communication, mixed-signal test, and frequency synthesis. He has worked as a consultant for SMEs and multinationals in the microelectronics industry and is founding Director of the Microelectronics Industry Design Association (MIDAS Ireland) and the Microelectronic Circuits Centre Ireland (MCCI). He won UCC's Invention of the Year Award in 2011 and led the development of the US-Ireland Research Innovation Awards in 2014/15. He was made a Fellow of the Institute of Electrical and Electronic Engineers (IEEE) in 1998 "for contributions to the theory of neural networks and nonlinear dynamics and for leadership in nonlinear circuits

research and education." He has served as Chair of the IEEE Gustav Robert Kirchhoff Award Committee and a member of the IEEE Fellows Committee. He has received many prestigious awards including Best Paper (International Journal of Circuit Theory and Applications), the 88th IEE Kelvin Lecture, IEEE Millennium and Golden Jubilee Medals, and the inaugural Royal Irish Academy Parsons Award in Engineering Sciences. In 2004, he was elected to membership of the The Royal Irish Academy and was made a Fellow of the Institution of Engineers of Ireland by Presidential Invitation. From 2005 to 2007, he was President of the European Circuits Society and Vice-President of the IEEE Circuits and Systems (CAS) Society (with responsibility for Europe, Africa and the Middle East). He was made a Fellow of the Irish Academy of Engineering in 2014. He was elected to membership of Academia Europaea in 2015. During 2012 and 2013, he was a Distinguished Lecturer of the IEEE CAS Society. He was elected Secretary for International Relations of the Royal Irish Academy in 2012. The following year, his RIA portfolio was expanded to include Policy. He was President of the RIA from 2017 to 2020.



Luca Avallone, PhD Student

Current Research: Advanced Frequency Synthesis

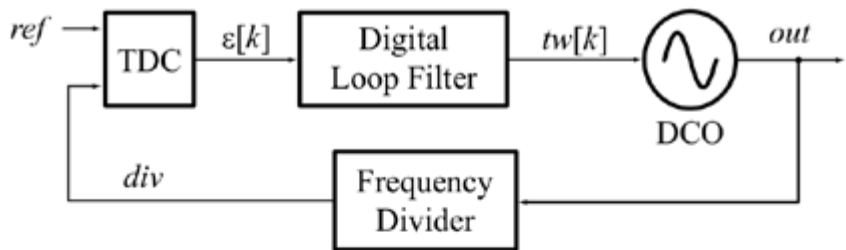
What's the area of your research?
Fractional-N All Digital PLLs.

The key points of the research are: understanding the state-of-the-art of the fractional-N structure identifying its main limits and problems; developing a theoretical analysis of fractional-N time-to-

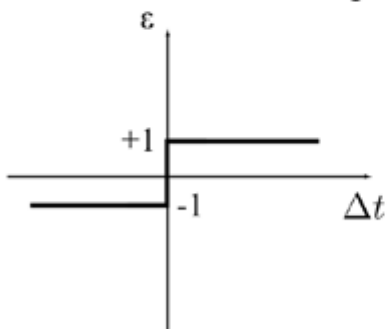
digital converter (TDC)-based Digital PLLs; implementing a new solution focusing on the TDC.

Education: Bachelor Degree in Electronic Engineering at University of Naples Federico II, 14/03/2014

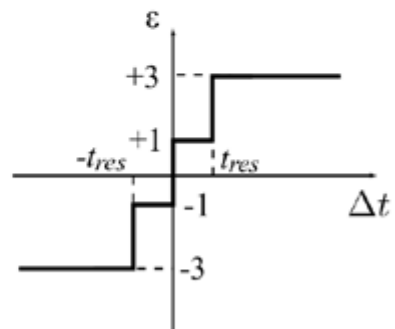
Master Degree in Electronic Engineering at University of Naples Federico II, 28/09/2017



All-digital PLL model



1-bit mid-rise TDC (binary phase detector) characteristic



2-bit mid-rise TDC characteristic



Dawei Mai, PhD Student

Current Research: High-Performance Fractional Frequency Synthesis

Modelling and analysis of the source of the spurious tones in the fractional-N frequency synthesis are always needed for achieving better communications systems. In the traditional phase-locked loop, the divider controller contributes significantly to the output phase noise. The conventional multi-stage noise shaping delta-sigma modulator divider controller (MASH-DDSM divider controller) with long input word length will induce periodic and time-varying spurious tones in the output phase noise spectrum. To understand the phenomenon, provide insight into the cause of it, and finally provide solutions to eliminate the periodic tones is the aim of the research.

Other components in the traditional analog and digital frequency synthesizers might pose performance limits to the performance of frequency synthesis. For example, the fractional input to the digitally controlled oscillator will introduce noise to the output phase noise. The exploration of those limits is another topic of the research.

Research Topics:

- Modelling of frequency synthesizers
- Spur elimination and noise reduction in fractional-N frequency synthesis

Education: Bachelor of Engineering (2015), University College Cork

Master of Engineering (2018), University College Cork



Salvatore Galeone, PhD Student

Current Research: RTWOs as multiphase oscillators for frequency synthesisers

The Rotary Travelling Wave Oscillator is an oscillator topology based on a transmission line rather than a lumped resonator. The RTWO operates by propagating a travelling wave along a differential transmission line that is closed in a Möbius connection. The losses of the transmission line are restored by distributed CMOS amplifier stages.

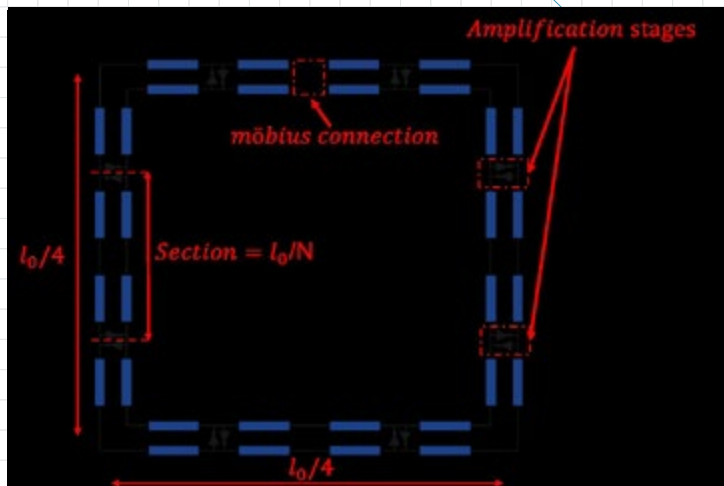
This oscillator topology is attractive for the intrinsic multiphase nature of the oscillator and its ability to operate a very high frequency with low phase noise and power consumption.

Research Topics: Oscillators, phase noise

Education: Salvatore holds a Bachelors' degree in Electronic Engineering from University of Pavia, Italy 2009

And Masters' degree in Electronic Engineering from University of Pavia, Italy, 2012

A rotary traveling wave oscillator is comprised of a Möbius connection of multiple sections of transmission line, with amplification stages in between to compensate for losses in the line.





Dr. Yann Donnelly, Post Doc Researcher

Current Research: Fractional-N Phase Locked Loops, which are employed throughout the communications industry, suffer from the appearance of spurious spectral components, “spurs”, which limit performance. This research topic has elucidated the causes of spurs and investigates novel techniques for reducing this unwanted behaviour. Work to date has achieved best-in-class measured spur performance and further improvements are being investigated.

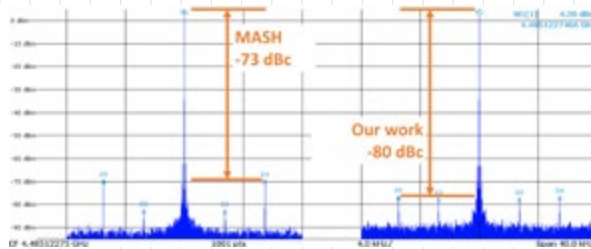
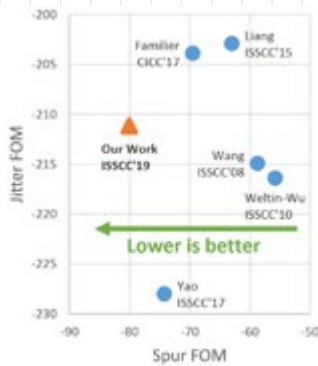
Research Topics:

- PLL phase noise spectrum prediction
- Reduction of fractional-N spurs by modulator redesign
- Silicon verification through digital IC implementation

Education:

BE (Electrical & Electronic) – University College Cork, 2014

PhD (Microelectronics) – University College Cork, 2018





Valerio Mazzaro, PhD Student

Current Research: Advanced fractional-N frequency synthesizers.

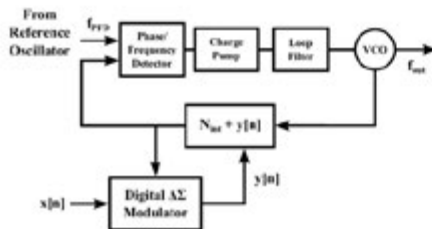
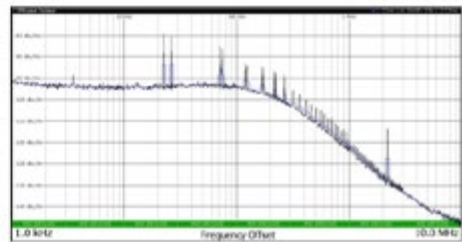
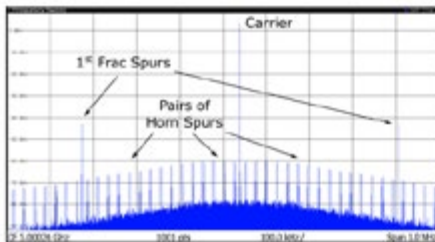
In fractional-N PLLs, increased phase noise and spurious tones come from the interaction between the DDSM quantization error and nonlinearities in the system.

The purpose of this project is to investigate the nature of spurious tones in fractional-N PLLs in order to predict them and, eventually, mitigate them.

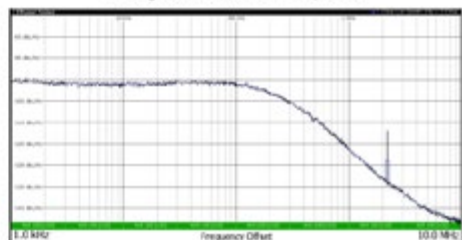
Research Topics: Frequency synthesis, fractional-N PLL design, phase noise, spurious tones, horn spurs.

Education: Bachelors Degree in Electronic Engineering at University of Naples Federico II, 2014

Masters Degree in Electronic Engineering at University of Naples Federico II, 2017



Mitigation of Horn Spurs





Xu Wang, PhD Student

Current Research: The CMOS device noise from the charge pump (CP) within the phase-lock loop together with other nonlinearity associated with the Fractional-N frequency synthesiser architecture induces spurious response and deteriorates the phase noise performance of the wireless communication system. The current research analytically studies the noise generation mechanism of the CP, the prediction of which is systematically compared with the system nonlinearity noise. Eventually the research aims to come up with novel CMOS

synthesiser design that optimally minimises the phase noise and spurs caused by both the device noise and system nonlinearity.

Research topics: System-and-block-level analogue design for advanced frequency synthesis, Machine-intelligence aided frequency synthesis.

Education: M.Eng. in Electrical and Electronic Engineering at Imperial College London (2015-2019)



Prof. Bogdan Staszewski

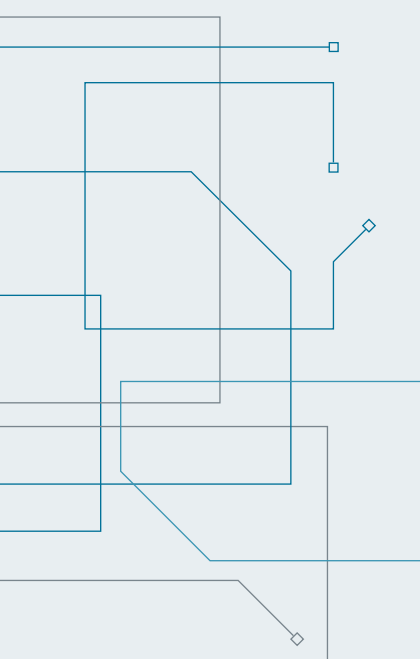
In Sept. 2014 Prof Staszewski joined University College Dublin (UCD) as a Professor while still holding a part-time Professor position at TU Delft. Prior to 2014, he was at Delft University of Technology (TU Delft) in the Netherlands, where he held academic positions since 2009. He joined TU Delft in 2009 after 18 years in industry with diverse experience in microelectronics and communication systems. He is an IEEE Fellow for contributions to the digital RF communications systems. In 2012, he won the prestigious IEEE Circuits and Systems Industrial Pioneer Award. He has co-authored three books, six book chapters, 170 journal and conference publications, and holds 140 issued US patents.

Professional experience: University College Dublin. Position Professor in the School of Electrical, Electronic & Communications Engineering. Carrying out research and teaching in the area of microelectronic circuit design; concentrating on frequency synthesis and RF using advanced CMOS for Internet-of-Things (IoT).

Delft University of Technology (TU Delft), Delft, the Netherlands. July 2009 to present. Carrying out research and teaching in the area of microelectronics, concentrating on frequency synthesis and RF using advanced CMOS.

From 1995 to 2009, he was with TI Dallas, where achievements included the invention and development of the Digital RF Processor (DRP) technology: A novel all-digital frequency synthesizer, all-digital RF transmitter and discrete-time RF receiver architecture that is suitable for the mainstream digital CMOS processes and presents a unique opportunity to build ultra low-cost and power-efficient single-chip radios. Developed a new digitally-intensive CMOS read channel architecture for magnetic recording hard-disk drives. Prior to TI he worked with Alcatel Network Systems, Texas from 1991 – 1995, included work in telecommunications systems, discrete analog and digital circuits, high-speed signal integrity, software algorithms.

Education: Ph.D. in Electrical Engineering, University of Texas at Dallas, USA. Thesis "Digital deep-submicron CMOS frequency synthesis for RF wireless applications," July 2002. M.S. in Electrical Engineering, University of Texas at Dallas, USA, with concentration in digital systems, Dec. 1992. B.S. in Electrical Engineering, Summa Cum Laude, University of Texas at Dallas, USA, with concentration in telecommunications, May 1991.





Reza Nikandish, Research Staff

Reza received his Ph.D. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2014. He is a Research Fellow with the University College Dublin, Ireland. Reza was a recipient of the Marie Curie Post-Doctoral Fellowship from the European Union's Horizon 2020 Research and Innovation Program from 2017 to 2020. He was also a recipient of the Iran's National Elites Foundation Fellowship from 2010 to

2014 and the Second-Place Award Winner of the National Electrical Engineering Olympiad in 2004.

His current research interests include:

- CMOS integrated circuits for quantum computing and sensing
- Energy-efficient AI and machine learning
- Integrated circuits for mm-wave communications



Amir Bozorg, Post Doc Researcher

Amir Bozorg has been a PhD student at UCD since February 2016. His thesis project is on "mm-wave/RF transceiver design". Between Feb. 2017 and Jan. 2019, he was a part-time R&D scientist at S3 Semiconductor, currently Adesto Technology, in Dublin, Ireland, where he developed a K-band phased array receiver. He has received his MSc degree from Amirkabir University of Technology

(Tehran Polytechnic), Tehran, Iran in 2012 in Microelectronics (with Hons.).

His research interests are:

1. Radio frequency/mm-wave transceiver design,
2. Discrete-time receiver and filter designs,
3. All-digital phase locked loops and frequency synthesizers,



Feifei Zhang, PhD Student

Current research GHz digital Cartesian RFDAC design

Research topics:

All digital modulator design;

Class E/F power amplifier design;

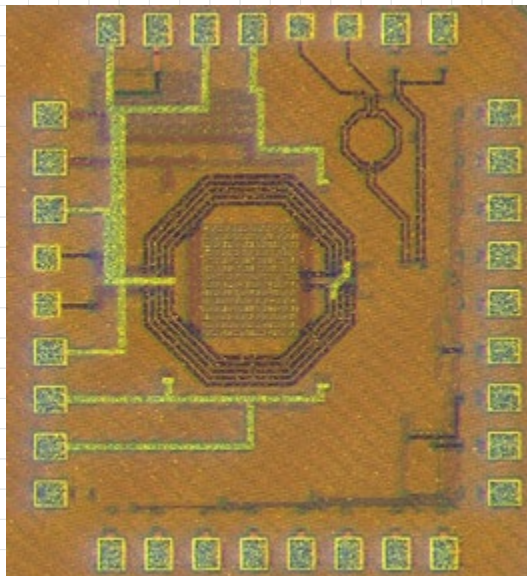
FPGA implementation

MSc of Microelectronics in Beijing University of Technology, China in 2014;

BSc of Navigation guidance and control in Beijing University of Aeronautics and Astronautics, China in 2011

Education:

Joined in Prof. Staszewski's group in Feb. 2017 UCD from Sep. 2014;

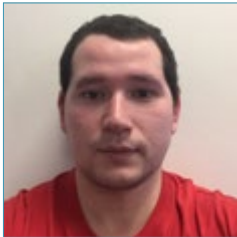




Dr. Panagiotis Giounanlis, Post Doc Researcher

Panagiotis Giounanlis is a postdoc researcher at UCD since September 2017. His current work includes the development of numerical and analytical approaches for the modeling and simulation of nano-structures and semi-conductor coupled quantum-dots, the development of circuit equivalent models for electron transfer through multiple-quantum-dots, the characterisation and modeling of CMOS devices operation at low temperatures and others. He received his B.SC. degree in Physics and M.Sc. degree - Computational

Physics Master of Science from Aristotle University of Thessaloniki (AUTH), Greece, in 2008 and 2011 respectively. In 2017, he received his Ph.D degree for his research on the modeling of non-linear effects for micro-scale devices (MEMS) and their application to reliability and control by the use of both numerical and analytical approaches. His research interests include: Modeling and simulation of micro/nano-scale devices and mixed-domain complex systems; Solid state Physics; Computational quantum mechanics.



Viet Anh Nguyen, PhD Student

Current Research: Viet Anh Nguyen is currently researching ultra-low-voltage, oscillator-based ADCs for Internet of Things applications.

Research Topics:

1. Analog and Mixed-Signal Integrated Circuit design,
2. Analog-to-digital converters,
3. Time-to-digital converters,
4. Process, voltage and temperature (PVT) tolerant ultra-low voltage design.

Education: Viet Anh Nguyen has been a PhD student at UCD since September 2017. He received his Masters degree in Electronic and Computer Engineering in 2017 and his Bachelors degree in Electronic and Communications Engineering in 2016, both from University College Dublin (UCD), Ireland.



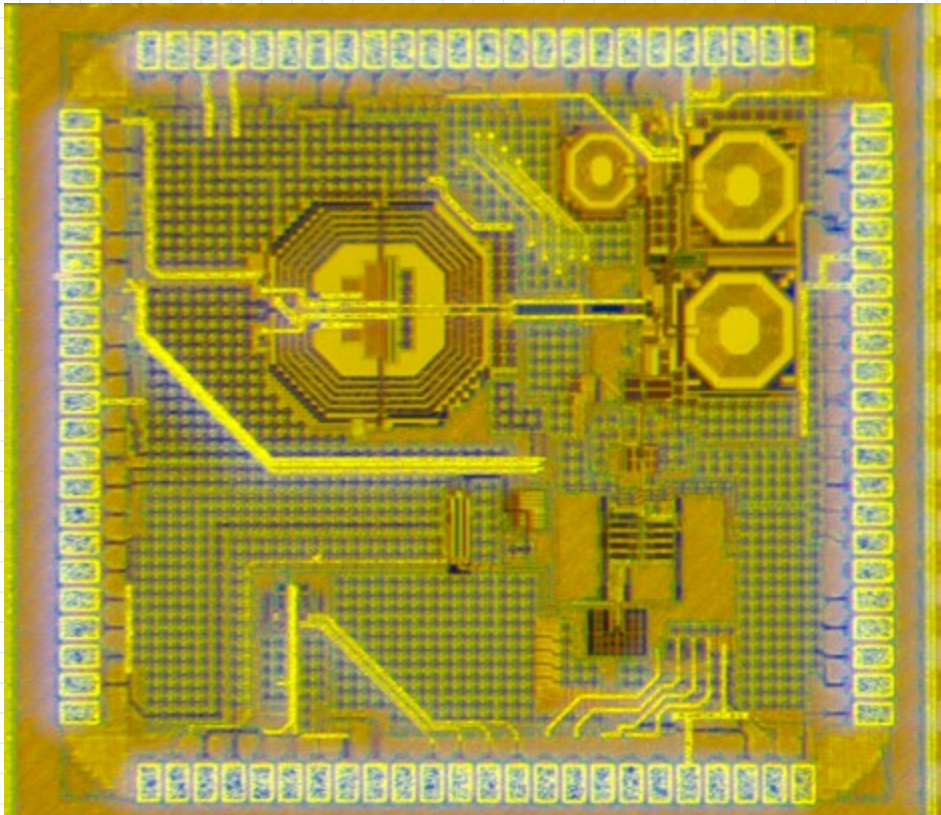
Suoping Hu, PhD Student

He was born in Changzhou, China. He received the B.E. degree in Integrated Circuit Design and System from Tianjin University (TJU), Tianjin, China, in 2013, and the M.Sc. degree (Hons.) in Electronic Science and Technology from Shanghai Jiao Tong University (SJTU), Shanghai, China, in 2016. He is currently pursuing the Ph.D. degree with University College Dublin (UCD), Dublin, Ireland. Since

2017, he has been sponsored by Analog Device, Cork, Ireland, and worked in a joint project -- ULP receiver.

His current interests include:

- Phase-tracking receiver design
- Ultra-low-power receiver design for BLE application.
- Discrete-time circuit design
- Analog/RF circuit design





Hongying Wang, PhD Student

Current Research: Digital-intensive low-power ADC design with the nanoscale CMOS technology for IoT application and Cryogenic circuit design for the Quantum computer.

Research Topics:

- Digital intensive Level Crossing Sampling ADC design
- Passive Delta Sigma ADC design
- Single Electron detector design for Quantum Computer
- Front-end circuit design for cryogenic application

Education: She received her MSc and BSc degrees in Microelectronics from Harbin Institute of Technology, Heilongjiang Province, China in 2015 and 2013, respectively. She is currently pursuing her PhD degree in Microelectronics at University College Dublin (UCD), Dublin, Ireland.



Yizhe Hu, Post Doc Researcher

Yizhe Hu received the B.Sc. degree (summa cum laude) in microelectronics from Harbin Institute of Technology (HIT), Harbin, China, in 2013, and the PhD degree in microelectronics from University College Dublin (UCD), Dublin, Ireland, in 2019. He is currently working as a postdoctoral researcher with Prof. R. Bogdan Staszewski in UCD. From 2013 to 2014, he was with Fudan University, Shanghai, China, where he was involved in RFIC design as a postgraduate

researcher. From May 2016 to Oct 2017, he was consulting for the PLL Group of HiSilicon, Huawei Technologies, China, designing 16 nm DCOs and ADPLLs. Since June 2018, he has been consulting for the Mixed-Signal Design Department, TSMC, for a new type of PLL design. His research interests include RF/mm-wave integrated circuits and systems for wireless communications. Dr. Hu has served as a frequent reviewer for the IEEE JSSC, TCAS-I/II, and TMTT.



Dennis M. Andrade Miceli, PhD Student

Current Research: Dennis Andrade-Miceli has been a PhD student at UCD since July 2016. His current research work is the framework of Quantum Computers particularly focused on FD-SOI devices modelling under cryogenic operation and ULP digital circuits. Other topics also covered along his research project are LDO, TDC, PVT compensation techniques, and Test automation. He received his MSc degree in Electronic Engineering in 2002 from National Institute of Astrophysics, Optics and Electronics (INAOE), Puebla, Mexico with the project Low-power pipelined ADCs. He received his BSc degree in Industrial Electronic Engineering from Veracruz Institute of Technology, Veracruz, Mexico, in 1998. He has held Electronic Engineering positions in Mexican Maritime Transportation (TMM); research staff in UCD and BarcelonaTech; and R&D Electronic Engineering positions in Arquimea, Intel Labs, and currently in Equal Labs.

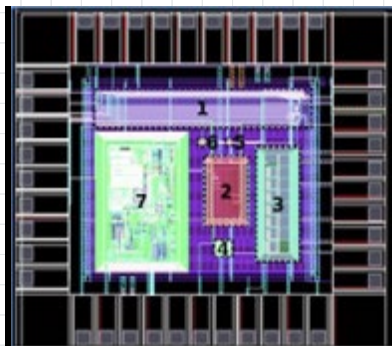
Research Topics:

- FD-SOI Modeling (BSIM, EKV, Verilog-A)
- Cryogenic Electronics
- Quantum Computing
- ULP (sub-Vt) Digital Circuits
- PVT compensation/mitigation on ULP digital circuits

Education: Ph.D. Candidate University College Dublin, Dublin, Ireland 2016 to present

Third level courses in Electronic Engineer Engineering and Junior Research Certification by Technical University of Catalonia, Barcelona, Spain. 2007 – 2011, 2013 – 2014

M.Sc. Electronic Engineering, National Institute of Astrophysics, Optics and Electronics. Puebla, México. 2000 – 2003 B.E.





Hieu Minh Nguyen, PhD Student

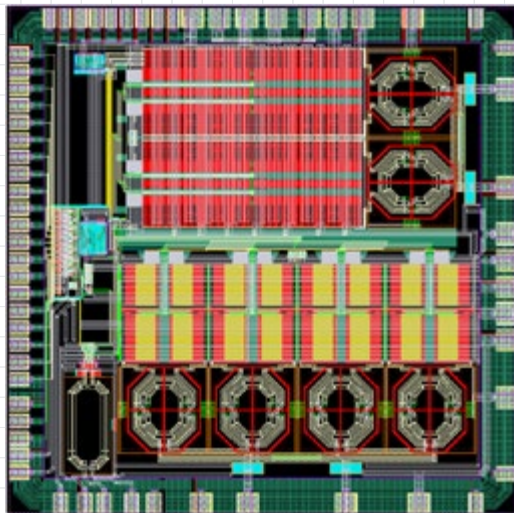
Current Research: Hieu Minh Nguyen is now focused on all digital RF Digital-to-Analog Converter and Transmitter for low-band and high-band 5G application.

Research Topic:

- Switched-Capacitor Power Amplifier (Switching Class)
- Hybrid Data Converter for Transmitter
- All Digital Charged Sharing RFDAC
- Power Combination network for high-efficiency Transmitter.
- mmW Digital Power Amplifier.

Education: Hieu M. Nguyen received the B.E. degrees, M.E in Electronics and Telecommunication Engineering from Ho Chi Minh City University of Technology in 2014 and 2016, respectively. During 2013–2014,

he joined Integrated Circuit Design Research and Education Center where he studied about Analog and RF integrated circuit design. He also received the Award of Best Student in Analog IC Design for the design of 24-Bit Delta Sigma ADC. From 2014 to 2015 he worked as a Teaching and Research Assistant at the Department of Electronics Engineering, Faculty of Electricals–Electronics Engineering, Ho Chi Minh City University of Technology. From 2015 - 2017 He worked as an Analog IC Design Engineer in Uniquify where he focused on the PHY and SERDES system. He is currently pursuing Ph.D. in IoE Laboratory in University College Dublin, his research is focusing on Digital Power Amplifier, RFDAC and RF integrated circuit design. He is also serving as a JSSC and TCAS reviewer.





Mohamed Shehata, PhD Student

Mohamed Shehata received his B.Sc. and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt in 2009 and 2016 respectively. He is currently pursuing his Ph.D. degree in microelectronics from University College Dublin, Dublin 4, Ireland. From 2009 to 2016, he was with MEMS Vision, Cairo, Egypt as analog/mixed-signal IC design engineer where he was involved in designing of VCOs and PLLs. In 2016, he joined Xilinx, Dublin,

Ireland as analog design engineer. Since 2017, he has been with Analog Devices, Limerick, Ireland as an RF design engineer. His current research interests include RF and millimeter-wave integrated circuits and systems for wireless communications and automotive radars. Mr. Shehata has served as a reviewer for the IEEE European Solid-State Circuits Conference (ESSCIRC) and IEEE International Symposium on Circuits and Systems (ISCAS) since 2017.



Ali Esmailian, PhD Student

Ali Esmailian was born in Isfahan, Iran, in 1990. He received the B.Sc. degree in microelectronics from the Isfahan University of Technology (IUT), Isfahan, Iran, in 2013, and the M.Sc. degree in microelectronics from the University of Tehran, Tehran, Iran, in 2016. He is currently pursuing the Ph.D. degree in microelectronics with the University College Dublin

(UCD), Dublin, Ireland. In 2017, he joined Equal1, California, USA, as an IC Design Intern.

His current research interests include:

- Time-based ADCs
- Cryogenic mixed-signal circuit design for quantum computer applications.



Jianglin Du, PhD Student

Current Research:

1. Design low-power oscillator, SAR-ADC for BLE application.
2. Design low-power wireless frequency synthesizer using reference-sampling digital phase locked loop.
3. Design grating coupler for silicon-photonics application.

Research Topics: Low-power PLL Design, low-power receiver system design.

Education: Jianglin Du received his MSc degree in Physical Electronics and BSc degree in Micro-Electronics from Jilin University, China in 2016 and 2013, respectively. He is currently pursuing his PhD in Mixed-signal Circuits Design for IoT at University College Dublin.



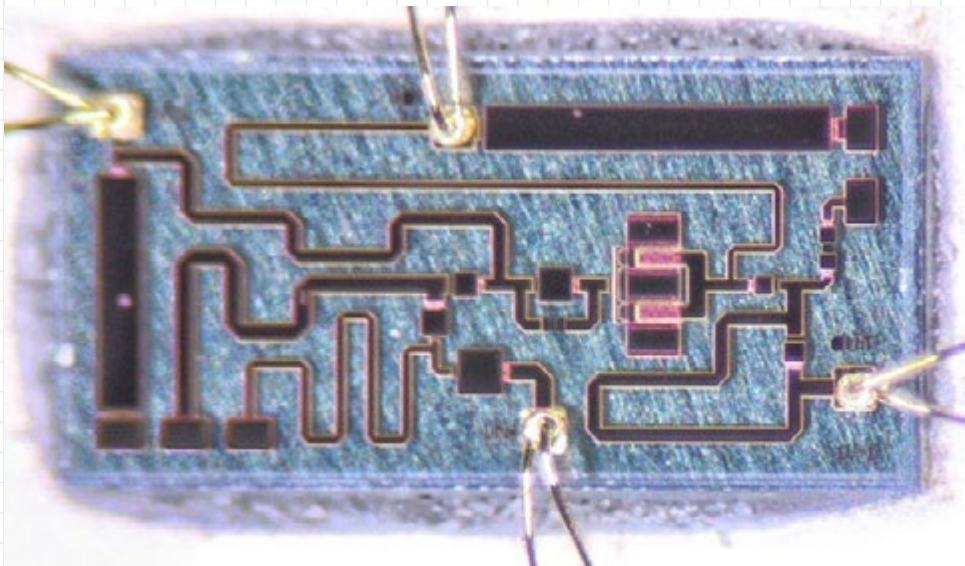
Yang Xu, PhD student

Current research: RF power amplifier design for 5G system and beyond, which offers efficiency enhancement at the power back-off and bandwidth extension at the same time.

Research topic:

- Broadband continuous mode power amplifier design
- GaN MMIC power amplifier for 5G system
- High efficiency power amplifier with enhanced performance

Education: She received her MSc and BSc degrees in Electromagnetic Field and Microwave Technology at Harbin Institute of Technology, China, in 2015 and 2013, respectively. She is currently pursuing her PhD degree in the RF & Microwave Research Group at University College Dublin (UCD), Dublin, Ireland.





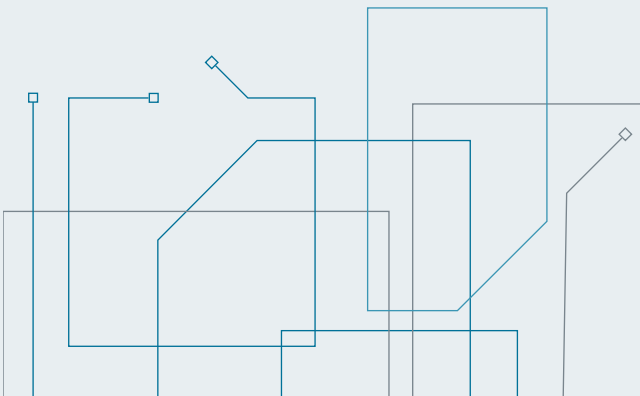
Prof. Anding Zhu

Anding Zhu received his Ph.D. degree in electronic engineering from University College Dublin (UCD) in 2004. He has been working in UCD since 2005, first as a Post-doc, then a Lecturer, an Associate Professor and now he is a Professor in the School of Electrical and Electronic Engineering. His research interests are in the area of nonlinear modelling and characterisation of RF circuits and systems with a particular emphasis on digital linearisation of RF power amplifiers for wireless communications. He has published over 100 peer-reviewed papers and received research funding from various sources including awards from Science Foundation Ireland (SFI), European Space Agency (ESA), Enterprise Ireland (EI) and industry donations.

Prof. Zhu collaborates with many universities and international companies. He was appointed as a Guest Research Fellow at University of Aveiro, Portugal in 2006 and worked as a Visiting Scholar at University of California at San Diego (UCSD) in 2007. Prof. Zhu

was undertaking a sabbatical leave working as a Visiting Assistant Professor at Stanford University from January to June 2013. He is currently with the RF & Microwave Research Group at UCD and he is the Director of the IoE2 Lab, a multi-disciplinary research laboratory focusing on developing enabling technologies and making scientific breakthroughs for next generation Internet of Things (IoT) and future (5G) communication networks. Prof. Zhu is a Funded Investigator in the SFI Research Centre for Future Networks and Communications - CONNECT, where he is particularly working on physical layer network-aware intelligent radio access nodes in collaboration with Xilinx, Analog Devices, MA-COM and Synopsys.

His current research includes behavioural modelling and digital linearisation of RF power amplifiers, high-frequency non-linear circuit and system simulation, wireless transmitter architectures, RF-DAC, digital signal processing and nonlinear system identification algorithms.





Mr. Brian Keogh, PhD Student

Current Research: Wideband Self Interference Cancellation for 5G Full-Duplex Radio.

Effective Self Interference Cancellation (SiC) is an important consideration for future 5G radio. If it can be successfully implemented, SiC has the potential to double spectral efficiency for certain 5G applications.

Research Topics: Fig. 1 Radio Architecture for Full-Duplex

Full-duplex operation is considered difficult to implement because the isolation between the transmit (TX) and receive path (RX) is not perfect. Current solutions take a

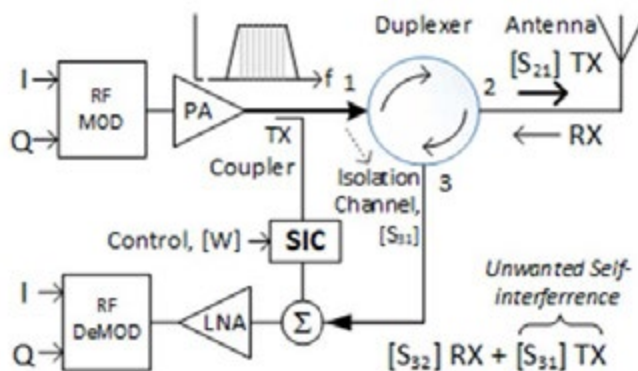
copy of the TX signal and use this copy to cancel the unwanted self-interference as shown Fig. 1.

The research topics focus on novel methods to extract time delayed copies of the TX signal so that advanced stochastic algorithms can precisely match the frequency domain response of the channel.

Education: BEng (Hons) in Electronic Engineering, MSc in Computer Science.

Lecturer in IT Tallaght, Department of Electronic Engineering.

Current PhD studies are supported by UCD and SFI.





Samaneh Sadeghi Maraht, PhD Student

Current Research: My research is mainly focused on designing small size antenna with high directivity/ gain and wide bandwidth that operates in the frequency of mm wave range (30 GHz-300 GHz).

Research Topics: mm-wave antenna for high speed data transmission

Education: University College Dublin

(Current PhD student), 2017-

K.N.Toosi University of technology (MSc), 2015

Guilan University (BSc), 2012



Chenhao Chu, PhD Student

Current Research: Chenhao Chu is focused on load modulated balanced power amplifier (LMBA) architectures with high efficiency and wide dynamic range over broad bandwidth for 5G communications.

Research Topics:

- Load modulated power amplifier design
- High-efficiency MMIC power amplifier design

Education: He received the B.E. degree from the Nanjing University of Science and Technology, Nanjing,

China, in 2015, and the M.S. degree (Distinction) from the City University of Hong Kong, Hong Kong, China, in 2017.

From Oct. 2017 to Sept. 2018, he was a Research Assistant with the State Key Laboratory of Millimeter Waves, Department of Electronic Engineering, City University of Hong Kong.

Currently, he is pursuing his Ph.D. degree in the RF & Microwave Research Group, at University College Dublin, Dublin, Ireland.



Enis Kobal, PhD Student

Current Research: Compact, low-loss, highly efficient transceiver components design for massive MIMO systems with CMOS technology.

Research Topics:

His research interests are:

- mm-wave transceiver components design for 5G MIMO systems including:
 - phase shifter design
 - power amplifier design
 - T/R switch design
- Characterisation and modelling
- mm-wave antenna design

Education:[2018 – 2022 (Expected)]
University College Dublin School of Electrical and Electronic Engineering
Doctor of Philosophy

[2013 – 2016] Middle East Technical University School of Electrical and Electronics Engineering Master of Science

Thesis Title: Comparative Design of Millimeter Wave RF-MEMS Phase Shifters

[2009 – 2013] Middle East Technical University School of Electrical and Electronics Engineering Bachelor of Science



Dr. Muhammad Usman

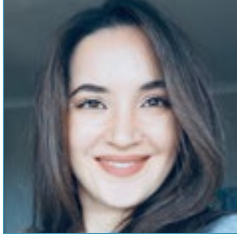
Introduction: Dr. Muhammad Usman has joined the RF & Microwave Research Group at University College Dublin (UCD), Ireland, in August 2019, as a Senior Research Fellow under EDGE Marie Skłodowska-Curie COFUND Action. His research interests are in the area of front-end antenna system design for wireless communication devices, RF circuit design and application of RF in biomedical Engineering.

Current Research: Currently, he is working on a project titled, "PAAS-5G, Spatially Polarized MIMO Phased Array Antenna Systems for 5G Wireless Communications". The main objective of this research is to design the innovative Multiple Input multiple Output (MIMO) phased array antenna systems for mobile phones and small cell base stations, operating at mid-band (24GHz-45GHz) with reduced mutual coupling and spatial correlation. Due to a large number of antenna elements integrated in a limited space, mutual coupling and spatial correlation become severe issues in 5G front-end design. In order to reduce the spatial correlation, this research will focus on innovative spatially polarized phased arrays. 2D and 3D phased arrays will be designed, to achieve the required beamforming for 5G. Reduced mutual coupling will be achieved by using meta material for designing

Dielectric Resonant Antennas (DRAs) with substrate integrated waveguide(SIW) transmission line technique for phase shifting. Furthermore, this research will be focusing on the use of ferrite materials as substrates to integrate large number of antennas in very compact manner, with reduced mutual coupling. A novel electronic circuit will be designed and integrated, to vary the incident magnetic field on ferrite substrates to achieve the required phase shift.

Education and Previous Experience:

Dr. Muhammad Usman had received his BSc in Electrical Engineering (Communication) from University of Engineering and Technology, Taxila, Pakistan in 2004 (Islamic International Engineering College, Islamabad). Later, he earned MSc and Ph.D in Radio Frequency Communication Engineering from University of Bradford, UK, in 2005 and 2009 respectively. Dr Usman joined University of Ha'il, Kingdom of Saudi Arabia, as Assistant Professor of Electrical Engineering in December 2009. He has been promoted to the rank of Associate Professor in Electrical Engineering at University of Ha'il, KSA in 2017. He has over nine years of teaching and research experience. He has contributed 35 international journals/conference papers.



Tugce Kobal, PhD Student

Current Research: Intelligent Digital-Calibration Algorithms for mm-wave Transceivers

Research Topics:

Her research interests are:

- Behavioural modelling of RF Power Amplifiers
- Linearization of RF Power Amplifiers
- Deep Learning Algorithms on Digital Predistortion

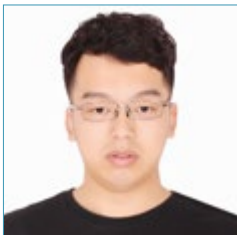
Education:

[2019 – 2023 (Expected)] University College Dublin School of Electrical and Electronic Engineering Doctor of Philosophy

[2014 – 2018] Middle East Technical University School of Electrical and Electronics Engineering Master of Science

Thesis Title: Dynamic Modelling and Control of a Gimballed Airborne Antenna Platform with Mass Unbalance and Friction

[2009 – 2014] Middle East Technical University School of Electrical and Electronics Engineering (Major) School of Psychology (Minor) Bachelor of Science



Xi Chen, PhD Student

My current research is mainly on millimeter-wave frequency synthesizers for 5G and beyond.

Education: Xi Chen received the B.E degree in information engineering from Southeast University, Nanjing, China, in 2018. From Sep. 2016 to June 2018, he was involved

with the design of the power amplifier in deep submicron CMOS technology, as a research intern, at the Institute of RF- & OE-ICs of Southeast University. In Sep. 2018, he joined RF & Microwave Group at University College Dublin, where he is currently pursuing his PhD degree.



Dr. Teerachot Siriburanon

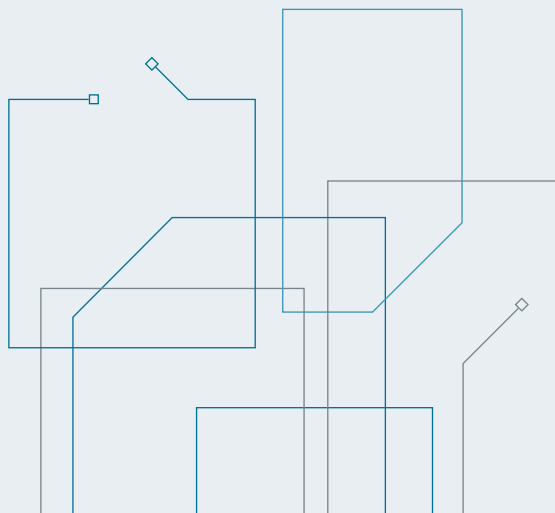
Teerachot Siriburanon received the B.E. degree in telecommunications engineering from the Sirindhorn International Institute of Technology (SIIT), Thammasat University, Pathum Thani, in 2010, and the M.E. and Ph.D. degrees in physical electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 2012 and 2016, respectively. In 2016, he joined University College Dublin (UCD), Dublin, Ireland, as a Post-Doctoral Researcher under the Marie Skłodowska-Curie Individual Fellowship Program. Since 2019, he has been an Assistant Professor with UCD.

Dr. Siriburanon was a recipient of the Japanese Government (MEXT) Scholarship, the Young Researcher Best Presentation Award at the Thailand– Japan Microwave in 2013, the ASP-DAC Best Design Award in 2014 and 2015, the IEEE SSCS Student Travel Grant Award in 2014, the IEEE SSCS Predoctoral

Achievement Award in 2016, and the Tejima Research Award in 2016. He has been a Guest Editor of the IEEE TRANSACTIONS ON CIRCUIT AND SYSTEMS–I in 2019-2020 and serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS.

Research Interests:

- Clock/frequency generations exploiting waveform technology, i.e. wave-locked loop, charge-sharing locking, reference waveform sampling
- Waveform-shaping for low-phase-noise oscillators
- mm-wave transmitter/receiver for 5G communications and beyond
- Mixed-signal circuits design for quantum computer and artificial intelligence.



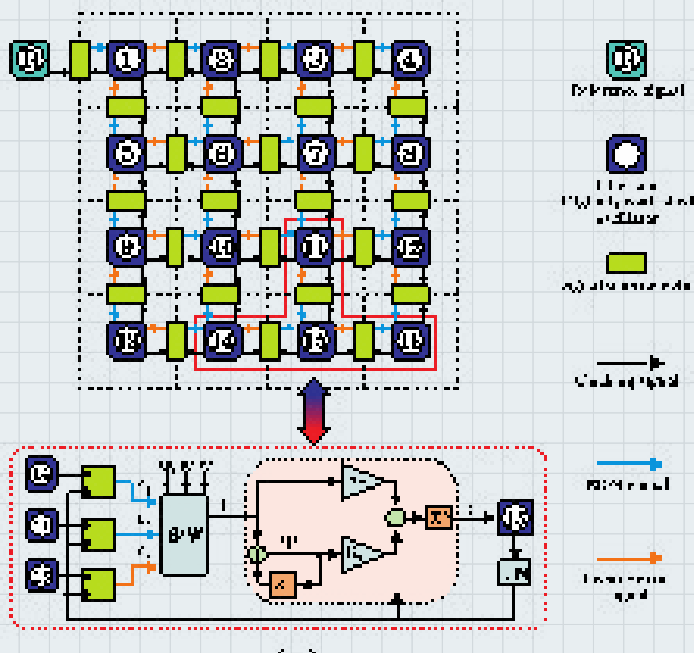


Dr. Elena Blokhina

Research areas: Emerging applications of circuits and systems and analytical and numerical methods for the design, analysis and simulation of multi-physics micro and nano-scale systems and quantum electronics. My research interests also include computer aided design and system verification.

Research topics: design and optimisation microelectromechanical energy harvesting systems, CMOS oscillator networks, CMOS quantum computers

Qualifications: Habilitation HDR (equiv. D.Sc.) degree in electronic engineering from UPMC Sorbonne Universities, France; the Ph.D. degree in physical and mathematical sciences and the M.Sc degree in physics from Saratov State University, Russia. Prof Blokhina is a Senior member of IEEE and the Chair of the IEEE Technical Committee on Nonlinear Circuits and Systems.





Dr. Deepu John

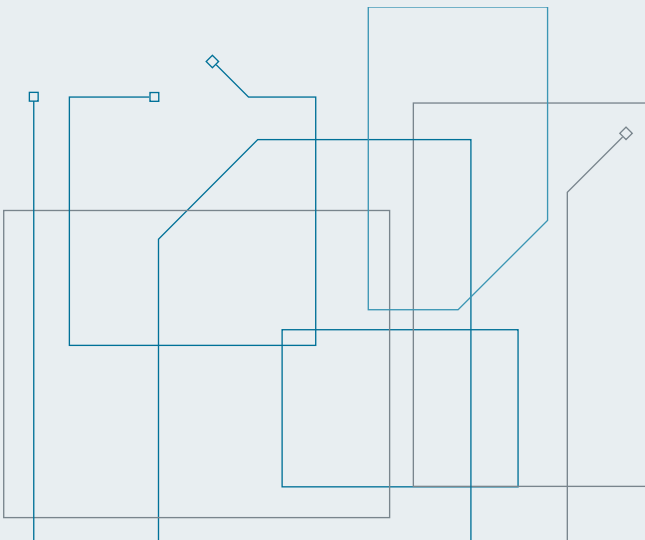
Deepu John is an Assistant Professor at University College Dublin. He is a recipient of Institution of Engineers Singapore Prestigious Engineering Achievement Award (2011), Best design award at Asian Solid-State Circuit Conference (2013), IEEE Young Professionals, Region 10 individual award (2013). He served as a member of technical program committee for IEEE conferences ASICON 2015, TENCON 2016, ICTA 2020. He is a reviewer of several IEEE journals and conferences. He serves as an Associate Editor for IEEE Transactions on Biomedical Circuits and Systems, Guest Editor for IEEE Transactions on Circuits and Systems and IEEE Open Journal of Circuits and Systems currently. His current research includes 1) Edge AI for IoT Biomedical devices 2) Distributed AI for wearable healthcare 3) Event driven AI for IoT devices 4) Multimodal data fusion for IoT sensors. He is a senior member of the IEEE.

Research Topic:

- AI for IoT devices
- Wearable Biomedical Sensors
- Biomedical Circuits and Systems
- Energy Efficient Signal Processing

Education:

- PhD in Electrical Engineering from National University Singapore (2014)
- MSc in Electrical Engineering from National University Singapore (2008)
- B. Tech in Electronics & Communication Engineering from University of Kerala (2002)





Guoxin Wang, PhD student

Current Research: The research here is on the implementation of ECG-based human authentication on embedded system. Previous work achieved a high accuracy result with convolutional neural network. However, the time and space complexity of those approaches is too high to be deployed in a wearable device. The research

focus is to use one-dimension signal and to combine it with low-complexity binary network that implement real-time authentication.

Research Topics: Continuous authentication using IoT sensor.

Education: Bachelor of Engineering, Beijing University of Technology, Beijing, China (2019)



Adnan Ashraf, Masters Student

Current Research: IoT Wearable Sensor Design; developing hardware and firmware of a low power ECG wearable device besides deploying the AI code to detect arrhythmia

Research Topics:

- Energy Efficient Embedded Systems

- IoT
- Wearables
- Wireless sensor networks

Education: 2009: B.Eng. in Electrical Engineering, from National University of Sciences and Technology, Pakistan



Gawsalyan Sivapalan, Masters Student

Gawsalyan is currently a M.Eng.Sc. Student / Researcher at University College Dublin. He received his B.Sc.Eng.(HONS) degree in Electronics and Telecommunication Engineering from the University of Moratuwa, Sri Lanka in 2016. He has also completed CIMA (Chartered Institute of Management of Accountants - UK) professional qualification. Previously, he has been working in research and business strategy development

sectors across corporate and startup companies in Sri Lanka.

His current research focuses on design and development of computationally efficient neural networks and machine learning methods for continuous monitoring of Electrocardiogram signals from a point of care device. The research will result in development of wearable solutions that make arrhythmia predictions in real time.



Maryam Saeed, PhD Student

Maryam Saeed is a PhD scholar at the University College Dublin and a Schlumberger Faculty for the Future Fellow. Her current research includes designing arrhythmia classifiers for low power circuits using event-driven ADCs, advanced signal processing and deep learning. She has previously worked on neural spike sorting for implanted brain circuits and EEG based biomedical applications.

She received her M.S. degree in Electrical Engineering from National University of Sciences and Technology, Islamabad and her B.S. in Telecommunication Engineering from the National University of Computer and Emerging Sciences, Lahore. She has also received training in EEG data acquisition and equipment handling at the NeuroPsychology Lab, University of Oldenburg, Germany.



Arlene John, PhD Student

Arlene is currently a Ph.D. student at University College Dublin. Her research focuses on the development of data fusion frameworks for ambulatory health monitoring. Continuous and proactive monitoring of vital health signs using wearable sensors, outside a lab-environment, is a very attractive method for health analysis these days. However, there are several challenges involved in making wearable sensors a reality. One of the major challenges is the low quality of the signals acquired due to motion artifacts, lack of robustness due to a node failure, etc. Data fusion has emerged as a solution that can achieve improved accuracy and specific inferences over that which can be obtained using a single sensor source, as it

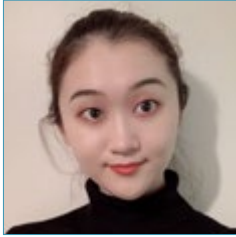
can enhance the performance of a task by combining information from multiple sensor sources.

Education: B. Tech, Electrical and Electronics Engineering from National Institute of Technology, Calicut

Research Interests: Biomedical signal processing, Algorithm design, Machine Learning, Robot-human Interaction and Behavioural Economics.

Experience: Worked at Bosch India ltd in engineering and strategy development for hybrid electric vehicles.

Research Intern at Indian Institute of Science, Bangalore with research focusing on statistical signal processing.



Li Xiaolin, PhD Student

Education: She received her BE (Electronics) degree from UCD and Beijing University of Technology in 2019. Her undergraduate major was Internet of Things (IoT). She is currently pursuing her Ph.D. degree with the Department of Electrical and Electronic Engineering, University College Dublin, Dublin, Ireland.

Research Interests: Continuous monitoring of vital physiological signals like Electrocardiogram (ECG), using wearable devices for early detection and preventive action is widely regarded as a solution to the costs and risks associated with cardiovascular disease. While the concept itself is not new, continuous monitoring of medical-grade physiological signals

has yet to become a reality. One of the major challenges involved is the high-power consumption of continuous wireless transmission, which makes the device too large for continuous use.

Her research aims to solve this problem by developing distributed machine learning technology, in which the preliminary classification of physiological signals is completed locally in the sensor and the rest is completed on the cloud server. Wireless transmission is enabled only when it is deemed necessary, based on initial processing. The topic is to develop powerful, accurate, fast and low-cost methods for identifying arrhythmia events in distributed wearable sensor data.



Mr. Seamus O'Driscoll, Principal Investigator

Current Research Focus: Leading teams across two main research strands, in Tyndall and in MCCI - in Integrated Power Systems and in Ultra-Low Power PMIC for IoT. The integrated power systems research is primarily centred on exploiting the opportunities being presented by recent advances in both thin film cobalt based magnetics-on-silicon (tf-MoS) and in substrate embeddable magnetic materials. The ultra-low power PMIC research is centred on the challenge of bringing advanced digital control techniques to the sub-micro watt PMIC arena. This will enable advanced feature set in next generation smart sensor nodes employing ambient energy harvesting and/or achieving extremely high battery life.

Research Activities:

- Highly integrated multi-level and multi-phase POL and iVR on 180nm SOI and 28nm Bulk CMOS. These employ inductor technologies spanning Co-Zr-Ta-B tf-MoS, substrate embeddable through to air-cored at 100MHz.
- Monolithically integrated GaN HEMT switching bridges and smart gate driver circuits, employing MoS functional level galvanic isolation.
- Ultra Low Power PMIC and power-centric SoC architectures, on 180nm CMOS, for smart sensing nodes at IoT edge and wearable.
- Integrated resonant converter systems.



Gerry Mc Glinchey, Senior Researcher

Current Research: (analog / mixedsignal) at MCCI, Tyndall National Institute, Cork, where he is investigating analog integrated circuits

Research Topics: Gerry's research interests are ultra-low power analog integrated circuits.

Current Research Focus: Ultra Low Power PMIC and associated mixed signal circuit design techniques

to create a variety of Nano power implementations of oscillators, charge pumps, dynamic precision references, extra low voltage cold start, DACs, ADCs, level shifting comparators and amplifiers.

Education: MSEE from Santa Clara University, California.

BE from National University of Ireland, Dublin



Ruaidhrí Murphy, PhD Student

Current Research:

- Depletion mode GaN HEMT based voltage regulator modules. GaN is a wide bandgap material capable of operating at high frequencies. GaN has the potential to reduce the footprint of voltage regulator modules for next generation electronics.
- Planar embedded inductors. Embedding the inductor within the substrate of a voltage regulator module has potential to reduce footprint and the manufacturing cost of the module. The inductor is an integral part of many power converter topologies. Research is based on analysing the

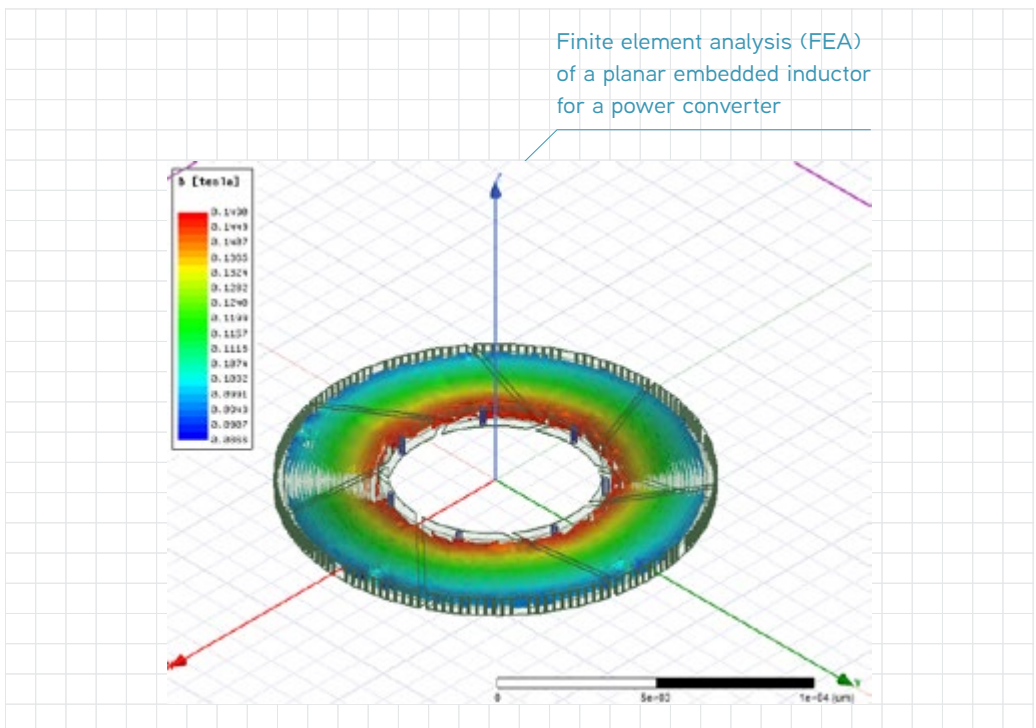
embedded inductor device and modelling it using FEA simulators such as Ansys Maxwell and Keysight ADS.

Research topics:

- Point-of-load converters
- Integrated magnetics
- Planar magnetics
- GaN HEMT
- Power electronics

Education:

- Presentation Brothers College Cork
- University College Cork (Beng Electrical and Electronic Engineering, PG Cert ICE)





Venkata Bhumireddy, Senior Research Engineer

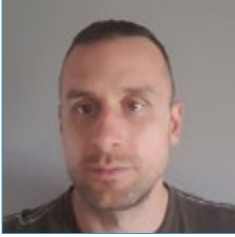
Current Research: Conversion efficiency of the DC-DC converter is very critical which demands low energy consuming analog circuits. Various buck converter circuits are being implemented to establish the benefit of high-side NMOS over PMOS at 100MHz. Current research work focuses on the design of ultra-low energy high precision 14bit ADC for dc-dc converters which can convert multiple analog input channels to digital output. Challenges in the research are to achieve higher accuracy and guaranteed monotonicity with high speed and low energy in 180nm technology.

Research Topics:

- Design of ultra-low power high precision Analog-to-Digital Converter (180nm CMOS)
- Design of high switching frequency, high efficiency dc-dc converters (iVR for SoC) with bootstrapped flying gate drivers (28nm CMOS).
- Design of high speed all digital-PLL with low jitter.

Education:

1. Bachelor of Science (B.Sc)
2. Master of Science (M.Sc)
3. Master of Technology (M.Tech)



Zoran Pavlovic, PhD Student

Highly integrated, flexible, multiple-output, point-of-load (POL), DC-DC power management module appropriate for providing all the standard internal system voltages required in the next generation battery powered smart devices.

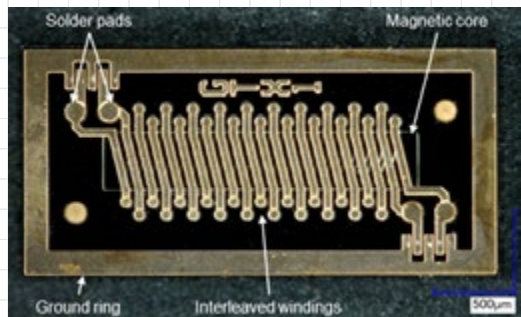
Research Topics:

- PMIC integrated power solution for PwrSiP application.
- Multi-level and resonant converter topologies.

- Thin film Magnetics-on-Silicon (tf-MoS) and PCB embeddable inductor technologies.
- 180nm SOI and 28nm CMOS implementations.
- 20MHz LLC Resonant Converter MoS isolated CMOS gate drivers.

Education: PhD in Power Electronics

PMIC (130nm CMOS) –
Synchronous Rectifiers and Gate
Drivers for 20MHz LLC Resonant





Madhu Jacob, PhD Student

Current Research: Power Management IC design for ultra-low power energy harvesting application.

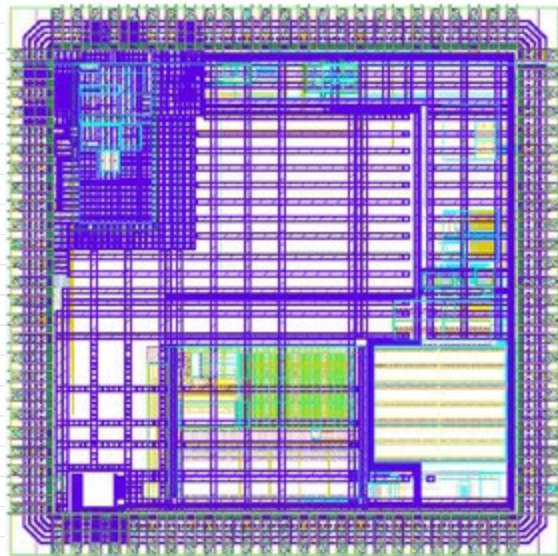
Research Topics: Power management IC: Successfully taped out power management IC for 1uW+ applications. This was used a buck-boost architecture to satisfy wide voltage range. Efficiency was above 90% for voltage range in energy harvesting applications. Designed, completed lay-outs and verified power-path and various analog control blocks using CAD tools. Designed and implemented digital blocks through full flow from Verilog to place-and-route with Cadence Innovus.

Low Voltage Cold Start design: This feature allows power management

ICs to start from low voltage. Simulated integrated circuit solutions using Tyndall fabricated thin film Magnetics-on-Silicon (MoS) transformer to achieve startup voltage from 30mV. This circuit was taped out and awaiting silicon samples. A new version of this circuit is in development to achieve 10mV startup. Both MoS and PCB embedded cold-start transformer technologies are being fabricated, characterized and electrically modelled.

Education: Master in Electronics design, University of Glasgow, Scotland.

Bachelor in Electronics and communication, Cochin University, Kerala, India.





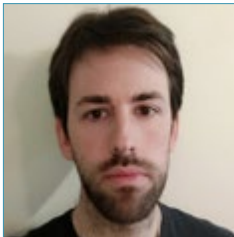
Brendan O Sullivan, PhD Student

Current Research: Investigation & design of isolated smart gate driver technologies. The gate drivers are being designed for implementation on 180nm SOI and are appropriate for Wide Band Gap (WBG) devices such as Gallium Nitride (GaN) High Electron Mobility Transistors (HEMT's) to achieve high frequency & high efficiency operation. Target applications include high step-down DC-DC Point of load converters operating directly from higher voltage systems, such as 48V automotive.

Research Topics:

- Smart Gate Driver Design
- Gallium Nitride High Electron Mobility Transistors – Device Modelling
- Closed Loop Control Systems
- Isolated Converter Systems

Education: Currently studying for a PhD



Andrija Stankovic, PhD Student

Current research: Ultra low power mixed-signal circuits, digital control loop design for power management circuits used in battery life extending and energy harvesting systems (180nm CMOS). Digital MPPT circuits and impedance matching control loops for transducers such as TEG and PV.

Research topics:

- Ultra low power digital circuits design
- Control systems characterisation and design

- Multi-disciplinary system modelling
- Power electronics, CMOS circuit design.

Education: I graduated from School of Electrical Engineering, University of Belgrade, Serbia with a Bachelor's degree in Electrical and Electronics Engineering and Computer Science. Two years later, in 2017, at the same university, I completed my Master's degree in Electronics Engineering.



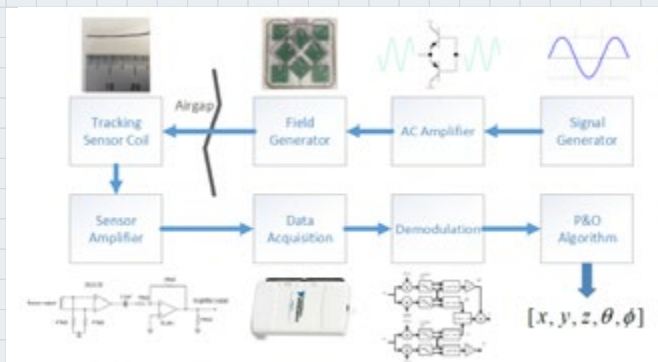
Dr. Pádraig Cantillon-Murphy

Has developed the first open-source electromagnetic tracking platform which can track medical instruments with sub-millimeter accuracy which we have chosen to make available free to the global research community (<http://anser.io>). Our next generation sensor technology will result from the current work at MCCI and we believe it will drive the platform to be commercially viable.

Education: He is a Senior Lecturer in Electrical and Electronic Engineering at UCC, academic member of Tyndall National Institute & honorary faculty at l'Institut de Chirurgie Guidée par l'Image in Strasbourg. He has a first-class honours B.E. degree in Electrical and Electronic Engineering from UCC and Masters of Science and Ph.D. degrees at the Department of Electrical Engineering and Computer Science at Massachusetts Institute of Technology (MIT).

From 2008 to 2010, he was a postdoctoral research fellow with concurrent appointments at Harvard Medical School, Brigham and Women's Hospital, Boston and at the Research Laboratory of Electronics at MIT. He is principal investigator at the Biomedical Design Laboratory at UCC and Tyndall National Institute which explores novel device development in image-guided surgery and endoscopy.

His current research interests include magnets for surgery, electromagnetic tracking and navigation and surgical robotics. He is module coordinator for the UCC Biomedical Design module, an award-winning teaching program which couples medical and engineering students at UCC. He is a former Marie Curie fellow (2010-2014), a former MIT Whitaker fellow (2007-08), and a senior member of the IEEE. He has co-founded two start-up companies and is co-inventor on 6 patent applications.





Herman Alexander Jaeger, Post Doc Researcher

Current Research: My work focuses on design and development of electromagnetic navigation systems for image-guided medical interventions. The core technology allows physicians to track the locations of medical instruments within the human body without the use of cameras or radiology.

Research Topics:

- Developing electromagnetic navigation systems for non-line-of-sight tracking applications
- Characterisation and design of magnetic sensors for tracked medical instruments
- Investigating tracking algorithm and system calibration methods.

Education: BEng Hons Electrical & Engineering, University College Cork, 2014

UROP internship in The Hamlyn Centre, Imperial College London, 2014

MEngSc Electrical & Engineering, University College Cork, 2015

PhD Electrical & Engineering, University College Cork, 2018



Dr. Kilian O'Donoghue, Research Fellow

Dr. Kilian O'Donoghue is an electronic engineer with over ten years experience in medical electronic design. Kilian has worked in multiple start-up and early stage medical device companies in Ireland and Canada, developing core technologies in robotics, sensing, navigation and medical imaging systems. His current research includes electromagnetic tracking systems, on-chip magnetic field sensors as well as large scale MRI hardware design.

Research topics: Electromagnetics simulations, magnetic field sensing technologies, electromagnetic tracking, data acquisition systems, medical devices

Education: Kilian graduated with a first-class honours B.E. degree (2011) in Electrical and Electronic Engineering, before completing his Ph.D in Electromagnetic Tracking Systems (2014), both from University College Cork.



Manish Srivastava, PhD Student

My current research focuses on design and development of Integrated Amplifier for electromagnetic tracking system for image-guided medical instrument. The sensor allows to track the locations of medical instruments within the human body. Before joining here, I have worked in companies (Qualcomm and Synopsys) in the field of Mixed

Analog circuit design and worked on high speed analog and digital circuit design. I also hold 4 issued and 5 filed US patents. Now, my interest in research and development propelled me to pursue a PHD in Data Converters and amplifier design.

Education: PHD Researcher in MCCI under supervision of Dr. Padraig Cantillon Murphy



Dr. Barry Cardiff

Current Research: Digitally-Assisted Analog Design
Embedded systems (mainly for biomedical devices)
Compressed sensing applications – currently focused on cost & power reduction of 5G systems.
Flexible waveforms for future wireless communications
Physical Layer Network coding in relay systems – design and analysis

Education:

- 2011: PhD Electronic Engineering from UCD.
- Thesis Title “Design Techniques for Vector Systems in Communications”
- 1995: M.Eng.Sc in Electronic Engineering from UCD.
- Thesis Title: “Digital Receiver Techniques in Mobile Communications”
- 1992: B.Eng in Electronic Engineering from UCD.



Mr. Armia Salib, PhD Student

Current Research: Digitally-Assisted Analog Design:

We are designing new methods to augment traditional ADCs with digital techniques in order to improve the overall circuit performance. This can result in smaller, cheaper, lower-power parts with equivalent conversion performance (e.g. ENOB), or conversely in high-end applications can allow very high conversion performance targets to be achieved. This work is being conducted in collaboration with local industry.

Research Topics:

Digitally-Assisted Analog Design

Education:

2014: M.Sc. in Electrical Engineering, from Ain Shams University, Egypt.

Thesis Title: Digital Calibration for Time Interleaved Analog to Digital Converter

2007: B.Sc. in Communications & Electronics, Alexandria University, Egypt.



Dr. Brendan Mullane

Brendan Mullane joined the University of Limerick (UL) in 2003, after spending more than 10 years in industry, mostly as a VLSI designer. He received his Ph.D. in Electronic Engineering from UL in 2010. His current role is Senior Research Fellow in the Dept. of Electronic and Computer Engineering. To-date, he has published over 35 peer-reviewed articles, authored one book-chapter, holds 10 invention disclosures and has been granted four US patents. His research interests include high performance, low-power VLSI signal processing, DSP/CPU and data converters applications.

Professional experience: Senior Research Fellow, Department of Electronic and Computer Engineering, University of Limerick. Carrying out research and supervision/teaching roles in the area of digital signal processing and VLSI design.

From 1992 to 1995, he worked with ALPS Electric (Fukushima/Japan) working on TV tuner electronics and C++ software design. From 1995 to 1996, he was with the start-up Silicon Systems Design (Dublin) developing DSP core IP for high-end audio applications. Prior to joining UL, he worked with the ASIC design company, LSI Logic (Tokyo/Japan) from 1996 to 2002 as a senior IC designer developing digital ICs for DVDs and other customer applications supporting ARM cores.

Research experience: During his time at UL, he has been Principal Investigator (PI) on a number of research projects involving data conversion and signal processing applications. He gained his Ph.D. in the area of data converter built-in-self test. He has received research-funding awards from Enterprise-Ireland and Science Foundation Ireland while also achieving various donations through collaborations with industry helping to train and graduate PhD/Masters researchers. Dr Mullane is also a Funded Investigator in the SFI Research Centre for Future Networks and Communications – CONNECT where he is working in collaboration with industry on advanced signal processing techniques to overcome noise sources in D/A converters.

He is currently with the circuits and systems research group at UL developing technology for next generation connected Internet of Things (IoT) devices that require safety critical signal monitoring capabilities. Current research include digital assisted signal-processing techniques for data converters, test and on-chip feature extraction and analysis. He is interested in the application of this research to areas such as integrated healthcare and brain monitoring devices.



Shantanu Mehta, Research Staff

Current Research: My current research is focused on dynamic element matching calibration techniques to overcome non-linear error sources in current-steering Digital to Analog Converters (DACs).

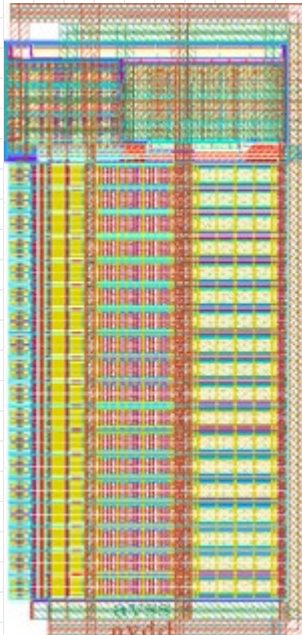
The aim is to increase the design performance using digital signal processing techniques attached to the analog D/A converter design. My research activities also included design of a tri-level current-steering D/A converter design for use in continuous time ADCs.

Research Topics:

1. High-speed ADC and DAC's.
2. Digital Signal Processing.
3. Sigma Delta ADC and DAC'S.
4. Dynamic Element Matching Techniques.

Education:

- Currently pursuing Ph.D. in Microelectronics from University of Limerick, Ireland.
- M. Tech, VLSI Design from Vellore Institute of Technology, India.
- B.E., Electronics & Telecommunications from Walchand Institute of Technology, India.





Fotios Kostarelos, MEng student

Current Research: My research is focused on developing a hardware system capable for detection of brain injuries by exploiting signal processing techniques and machine learning principles.

My research activities includes embedded hardware and FPGA high-level code development.

Research Topics:

1. Feature extraction.
2. Digital Signal Processing.
3. HLS coding.
4. Machine-learning

Education:

- Currently pursuing MEng in from University of Limerick, Ireland.
- BE/MTech, Electronic Eng. from University of Crete, Greece.



Dr. Darren Francis Kavanagh

Darren is a Lecturer, Principal Investigator & Programme Director for BEng Electronic Engineering with the Institute of Technology Carlow. He received his PhD degree in acoustic signal processing and machine learning (ML) methods from Trinity College Dublin, in 2011. Following this, Darren was a Postdoctoral researcher with the University of Oxford, UK. He has gained valuable academic teaching experience at the University of Oxford; Trinity College Dublin; and the Technological University Dublin. Darren also benefits greatly from industrial experience at Alcatel Lucent-Bell Laboratories, Intel, and Xilinx. He was awarded an EMBARK Scholarship (IRC) in 2006-2010 and the Minister's Silver Medal for Science from the Minister for Education (Ireland) in 2005.

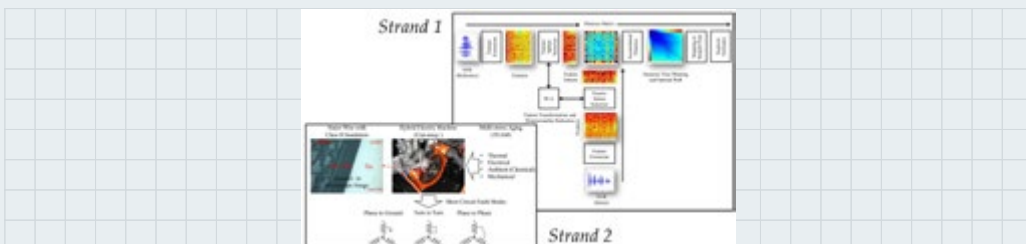
Darren has a strong track record of working closely with enterprise partners on applied RDI projects typically involving applied embedded systems for solving industrial engineering problems. Broadly, his research interests encompasses 'signals and systems' and can be defined under two main research strands: (1) signal processing and machine learning (ML) methods,

and (2) advanced Condition based Monitoring (CbM) of energy conversion and propulsion systems using low-cost and low-power embedded systems.

Core research aims:

- Design signal processing and machine learning ML algorithms for classification, segmentation and localisation to advance autonomous and intelligent systems.
- Fundamental research questions on degradation and fault modes of energy conversion systems, with applications in electric vehicles, renewables and medical devices.
- Development of low power embedded systems for novel electronic devices, systems, machines and equipment, utilising various Internet of Things (IoT) platforms.

Projects funded by EI; IRC; SFI, SEAI, Campus France and various collaborative industry partners. Currently interested in applied embedded systems for industrial applications and developing industrial-academic partnership opportunities.





Cian Madigan, PhD Student

Research Title: Cold Atmospheric Plasma Deposition of Biomolecules using Radio-Frequency (RF) Power Generators

Research Goals:

- Advance existing knowledge and understanding of the cold atmospheric plasma deposition process;
- Explore suitable non-intrusive laboratory methods for monitoring, measurement and characterisation of RF plasma using electronic sensing apparatus;
- Optimise the parameters of the deposition system for high performance, accuracy and repeatability,

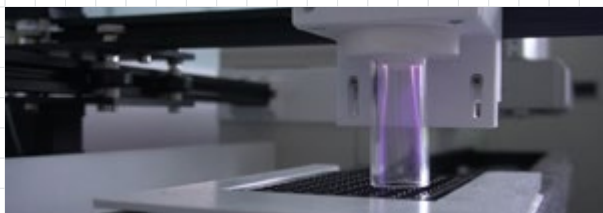
Current Research: My research involves conducting original applied electro-mechanical experiments in the laboratory, coating characterisation measurements, and parameterisation of the cold atmospheric RF plasma deposition system. BioDep is a coating process that was developed over a period of 10 years to attach drugs and biologics onto implant surfaces by Theradep Ltd. Arising out of plasma technology that was initially created for the textile industry, it has been

developed to bond materials to implant surfaces and labware. When applied to an implant surface, the plasma can sterilise, clean and produce chemical bonding sites on the metal or polymer surfaces. The therapeutic materials are then sprayed onto the reactive implant surface where they instantly cure to form a thin film coating. This novel electro-mechanical coating device will require novel non-intrusive electronic based sensing to optimise an extremely sensitive process.

Research Topics:

- RF Powered Cold Atmospheric Plasma Devices
- Applied Research in Plasma Medicine for Wound Healing
- Proof of Concept Designs and Experiments with Electro-Mechanical Apparatus
- Non-intrusive Electronic Sensing and Monitoring of the Plasma Process

Education: Bachelor (Hons) Engineering Degree with First Class Honours in Mechanical Engineering, Institute of Technology Carlow. 2018





Eoghan Chelmiah, PhD Student

Research Area: Advanced Machine Learning (ML) Methods for Energy Conversion Systems

Research Title: “Machine Learning Methods for Electric Machines used in Electric Propulsion Systems”

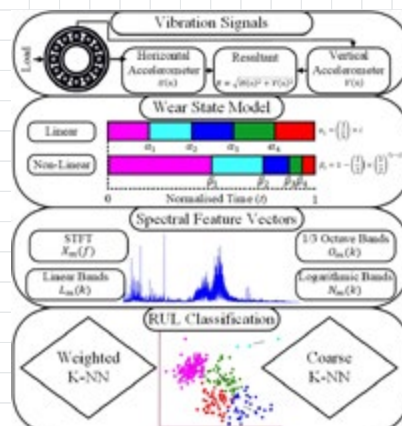
Research Goals: Developing new knowledge and understanding for the advancement and design of robust electric machines that prevents premature aging occurring and unexpected catastrophic failure modes occurring in critical applications and systems.

Current Research: My research is primarily based around investigating and developing novel methods of failure diagnostics and prognostics for industrial electric machines, using data-driven machine learning approaches. My work focuses on improving and optimising advanced Condition based Monitoring (CbM) methods for future generation electric propulsion systems.

Research Topics:

- Remaining Useful Life (RUL) estimation for rotating machines by performing a time-frequency analysis on vibration signals from accelerometers
- Investigating novel methods of feature extraction and classification using a combination of supervised and unsupervised Machine Learning (ML) approaches.
- Novel sensing approaches, analogue front end (AFE) circuits and state of the art System on Chips (SoC) for applied embedded systems.

Education: First class B.Eng (Hons) degree in Electronic Systems Engineering from the Institute of Technology Carlow in 2019.

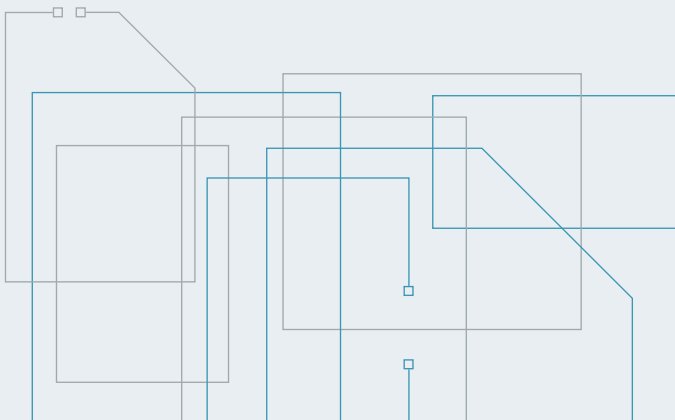




Dr. Emanuel Popovici

Emanuel Popovici (SM-IEEE, M-ACM) is a Senior Lecturer in Electrical and Electronic Engineering at University College Cork (UCC). Emanuel received a Dipl. Ing. Degree in Computer Engineering (with a major in Hardware Design) from the University Politehnica Timisoara, Romania in 1997 and a PhD in Microelectronics from University College Cork (National Microelectronics Research Centre) in 2002 respectively. Between 1997 and 2001 he did his research on efficient algorithms and hardware architectures for finite field arithmetic and error control coding within the National Microelectronics Research Centre, Ireland. Emanuel is the director of the award winning Embedded Systems@UCC research group (motto of the group is Engineering Inspired by Life). The group has built a distinguished publishing record of more than 200 papers on coding and cryptography algorithms and architectures, ultra-low power arithmetic, EDA for digital circuits, security and reliability in the context of SoC/NoC and in wireless embedded systems,

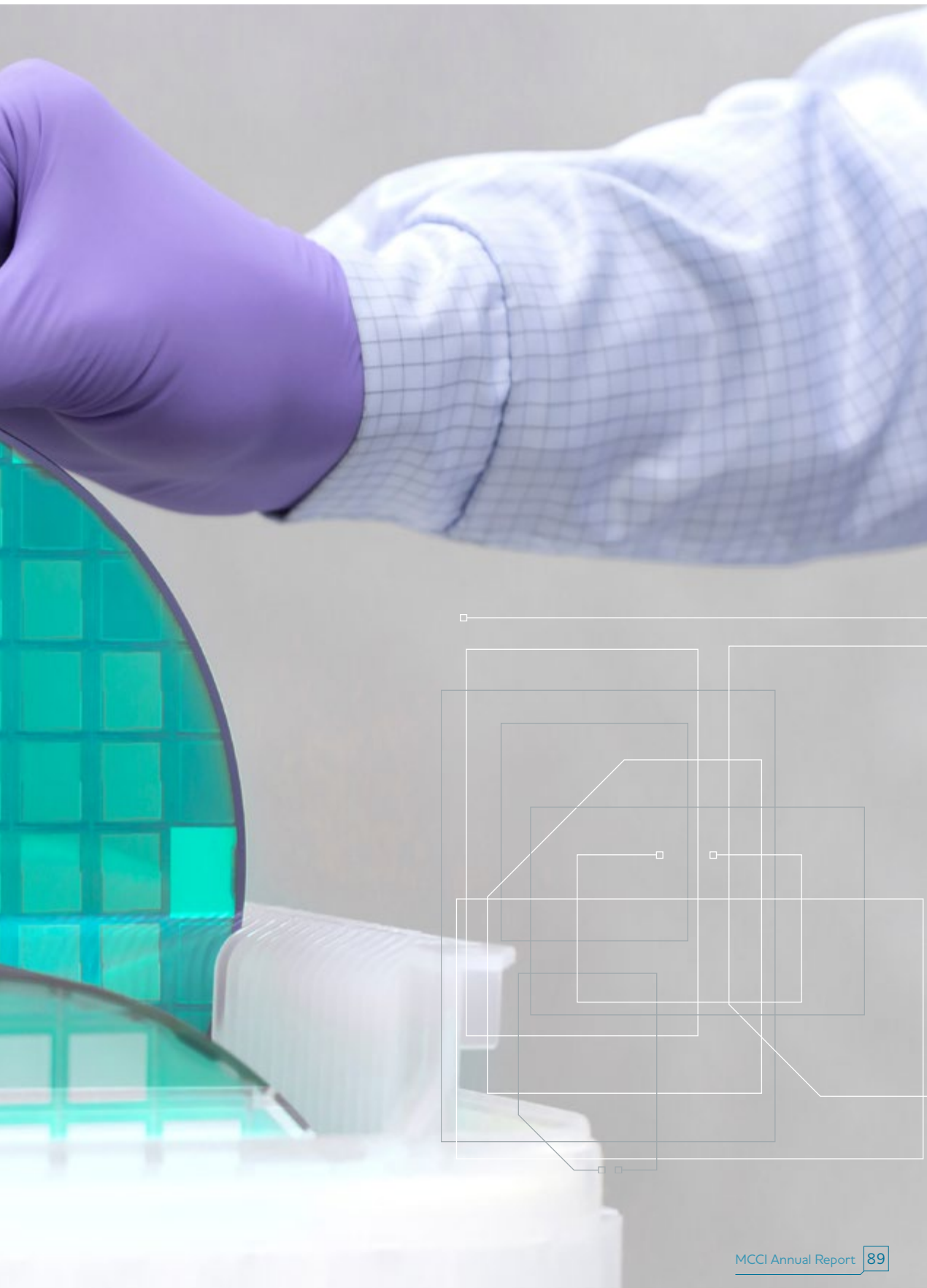
including sensor networks (WSN). Taking a truly interdisciplinary approach in research, the group has received more than 30 national and international awards and distinctions from organisations including IEEE, ACM, IET, MIDAS Ireland, IBM, Irish Lab Awards, etc. He mentored student teams who won 3 prizes in the prestigious IEEE/IBM Smarter Planet Challenge (first prize in 2011 project iCARE: improved healthcare for disadvantaged communities, second prize in 2013 project U-Play: unified networks and interfaces for playing with toys, first prize in 2014 project To Bee or not to bee=TRUE: from the beehive to the cloud and back). In 2016 his group received the Irish Engineering Lab of the Year award and in 2018 he received the Collaboration achievement award (Brain Stethoscope project together with INFANT Centre, Embedded Systems@UCC and Tyndall)



ALUMNI

Jason Hannon	2012	Yan Guo	2017
Jan Kubik	2012	Kevin McGrath	2017
Ray Foley	2012	Noel Kelly	2017
Aidan Keady	2012	Yuting Wei	2017
Lorenzo Mereni	2013	Valerio Marotta	2017
Vamshi Manthena	2014	Muhammad Asfand Awan	2017
Maurice Egan	2014	Shiyu "Steve" Zhou	2017
Lei Guan	2014	Hongjia Mo	2017
Greg Szczepkowski	2015	David Quilligan	2017
Diarmuid Collins	2015	Anil Jain	2017
Alberto Gola	2015	Mario Conti	2017
Francesco Brandonisio	2015	Cian O'Mahony	2017
Rishi Singh	2015	Karine Mnatsakanyan	2018
Mark Barry	2015	Mahsa Keshavarz Hedayati	2018
Hsin-Ta Wu	2015	Alberto Dicaldo	2018
Colm Murphy	2015	Anu Pillai	2018
Khosrov Sadeghipour	2015	Kathy Hanley	2018
Giuseppe Macera	2016	Pedro Paro Filho	2018
Girish Waghmare	2016	Ian Assom	2018
Ken Ahern	2016	Savatore Galeone	2018
Charles Perumal	2016	Filippo Schembari	2019
Jianghai He	2016	Mark Smyth	2019
Dimitris Kyritsis	2016	Vaibhav Pavnaskar	2019
Sohail Asghar	2016	Sean Philips	2019
Sohaib Afridi	2016	Stefano Facchin	2019
Andrew Malone	2016	James McCarthy	2019
Mengsu Yang	2016	Jeff Waling	2019
Niamh Costello	2016	Armia Salib-Farag	2019
Paolo Scognamiglio	2017	Naser Pourmousavian	2019
Stefano Tulisi	2017		

RESEARCH PUBLICATIONS



MCCI RESEARCH PUBLICATIONS

Highlight Publications

1. H. Wang, F. Schembari, and R. B. Staszewski, "An event-driven quasi-level-crossing delta modulator based on residue quantization," (JSSC), Nov 2019
2. Chen P, Zhang F, Zong Z, Hu S, Siriburanon T, Staszewski RB, "A 31- μ W, 148-fs Step, 9-bit Capacitor-DAC-Based Constant-Slope Digital-to-Time Converter in 28-nm CMOS", (JSSC), Nov 2019
3. Li M, Pang J, Li Y, Zhu A, "Ultra-Wideband Dual-Mode Doherty Power Amplifier Using Reciprocal Gate Bias for 5G Applications", (MTT) Oct 2019
4. G. Nikandish, R. B. Staszewski, and A. Zhu, "Broadband fully integrated GaN power amplifier with embedded minimum inductor bandpass filter and AM-PM compensation," (ESSCIRC), Sep 2019
5. H. Wang, F. Schembari, and R. B. Staszewski, "Passive SC $\Delta\Sigma$ modulator based on pipelined charge-sharing rotation in 28-nm CMOS," (TCAS-I), Aug. 2019
6. K. Xu; F. Kuo; H. R. Chen; L. Cho; C. Jou; M. Chen; R. B. Staszewski "A 0.85mm² 51%-Efficient 11-dBm Compact DCO-DPA in 16-nm FinFET for Sub-Gigahertz IoT TX Using HD2 Self-Suppression and Pulling Mitigation", (JSSC) 2019
7. A. Salib; M. F. Flanagan; B. Cardiff, "A Generic Foreground Calibration Algorithm for ADCs with Nonlinear Impairments", Vol 66, Issue 5, (TCAS-I), May 2019
8. A. Salib; M. F. Flanagan; B. Cardiff, "A High-Precision Time Skew Estimation and Correction Technique for Time-Interleaved ADCs", (TCAS-I), 2019
9. Y. Donnelly; M. P. Kennedy "Prediction of Phase Noise and Spurs in a Nonlinear Fractional-N Frequency Synthesizer" (TCAS-I), July 2019
10. J. Du, Y. Hu, T. Siriburanon, and R. B. Staszewski, "A 0.3 V, 35% tuning-range, 60 kHz 1/f³-corner digitally controlled oscillator with vertically integrated switched capacitor banks achieving FoMT of -199 dB in 28-nm CMOS," (CICC), Apr. 2019
11. Y. Donnelly, M. P. Kennedy, "Wandering Spurs in MASH 1-1 Delta-Sigma Modulators", (TCAS-I), 2019
12. M. P. Kennedy, Y. Donnelly, J. Breslin, S. Tulisi, S. Patil, C. Curtin, S. Brookes, B. Shelly, P. Griffin, M. Keaveney, "4.48GHz 0.18 μ m SiGe BiCMOS Exact-Frequency Fractional-N Frequency Synthesizer with Spurious-Tone Suppression Yielding a -80dBc In-Band Fractional Spur", (ISSCC), Feb 2019
13. P. Chen, X. Huang, Y. Chen, L. Wu, R. Staszewski. "An On-Chip Self-Characterization of a Digital-to-Time Converter by Embedding it in a First-Order $\Delta\Sigma$ Loop", IEEE Transactions on Circuits and Systems I (TCAS-I) Aug 2018
14. N. Pourmousavian, F.W. Kuo, T. Siriburanon, M. Babaie, R. Staszewski. "A 0.5-V 1.6-mW 2.4-GHz Fractional-N All-Digital PLL for Bluetooth LE with PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28-nm CMOS", IEEE Journal of Solid-State Circuits, Vol 53 Issue 9, Sep 2018 (JSSC)
15. Y. Hu, T. Siriburanon, R. Staszewski. "A Low-Flicker-Noise 30-GHz Class-F23 Oscillator in 28-nm CMOS Using Implicit Resonance and Explicit Common-Mode Return Path", IEEE Journal of Solid-State Circuits, July 2018 (JSSC)
16. D. Mai and M.P. Kennedy. "A Design Method for a Nested MASH-SQ Hybrid Divider Controller for Fractional-N Frequency Synthesizers", IEEE Trans. Circuits and Systems-Part I, 65(*): April 2018. (TCAS-I)
17. O'Connell, I, and O'Riordan, (2018) "Techniques for reducing ULP device power

- consumption”, Industry Session 5: Energy Harvesting, APEC, Mar 2018
18. Y. Li ; W. Cao ; A. Zhu, “Instantaneous Sample Indexed Magnitude-Selective Affine Function-Based Behavioral Model for Digital Predistortion of RF Power Amplifiers”, (MTT), 2018
 19. W. Cao, Y. Li, and A. Zhu, (2017) “Digital Suppression of Transmitter Leakage in FDD RF Transceivers: Aliasing Elimination and Model Selection,” IEEE Transactions on Microwave Theory and Techniques, Vol. 65, early access, Dec. 2017 (MTT)
 20. Kelly, N. and Zhu, A. (2017) ‘Direct Error-Searching SPSA Based Model Extraction for Digital Predistortion of RF Power Amplifiers’. IEEE Transactions on Microwave Theory and Techniques, 65 (MTT)
 21. Wang, H., Li, G., Zhou, C., Tao, W., Liu, F., and Zhu, A. (2017) ‘1-bit Observation for Direct-Learning-Based Digital Predistortion of RF Power Amplifiers’. IEEE Transactions on Microwave Theory and Techniques, 65 (07):2465-2475. (MTT)
 22. Cao, W., and Zhu, A. (2017) ‘A Modified Decomposed Vector Rotation-Based Behavioral Model With Efficient Hardware Implementation for Digital Predistortion of RF Power Amplifiers’. IEEE Transactions on Microwave Theory and Techniques, 65 (07):2443-2452 (MTT)
 23. Cao, W., Li, Y., and Zhu, A. (2017) Magnitude-Selective Affine Function Based Digital Predistorter for RF Power Amplifiers in 5G Small-Cell Transmitters 2017 IEEE MTT-S International Microwave Symposium (IMS) Honolulu, Hawai’i, USA, June 2017
 24. Y. Hu, T. Siriburanon, R. Staszewski, “A 30-GHz Class-F23 Oscillator in 28nm CMOS Using Harmonic Extraction and Achieving 120 kHz 1/3 Corner”, (ESSCIRC) Sept 2017
 25. H. Mo and M.P. Kennedy. “Masked Dithering of MASH Digital Delta-Sigma Modulators with Constant Inputs using Multiple Linear Feedback Shift Registers”, IEEE Trans. Circuits and Systems-Part I (TCAS-I), June 2017
 26. F. W. Kuo, N. Pourmousavian, T. Siriburanon, R. Staszewski, “A 0.5V 1.6mW 2.4GHz Fractional-N All-Digital PLL for Bluetooth LE with PVT-Insensitive TDC using Switched-Capacitor Doubler in 28nm CMOS,” IEEE Symposium on VLSI Circuits, June 2017
 27. H. Mo and M.P. Kennedy. “Masked Dithering of MASH Digital Delta-Sigma Modulators with Constant Inputs using Linear Feedback Shift Registers”, IEEE Transactions on Circuits and Systems I (TCAS-I), 2016
 28. Xia, J., Yang, M., Guo, Y., and Zhu, A. (2016) ‘A Broadband High-Efficiency Doherty Power Amplifier with Integrated Compensating Reactance’. IEEE Transactions on Microwave Theory and Techniques, 64 (07):2014-2024. (MTT)
 29. Yang, M., Xia, J., Guo, Y., and Zhu, A. (2016) ‘Highly Efficient Broadband Continuous Inverse Class-F Power Amplifier Design Using Modified Elliptic Low-Pass Filtering Matching Network’. IEEE Transactions on Microwave Theory and Techniques, 64 (05):1515-1525. (MTT)
 30. Kelly, N., and Zhu, A. (2016) ‘Low Complexity Stochastic Optimization-Based Model Extraction for Digital Predistortion of RF Power Amplifiers’. IEEE Transactions on Microwave Theory and Techniques, 64 (05):1373-1382. (MTT)
 31. Yu, C., Sun, H., Zhu, X., Hong, W., and Zhu, A. (2016) A Channelized Sideband Distortion Model for Suppressing Unwanted Emission of Q-band Millimeter Wave Transmitters 2016 IEEE MTT-S International Microwave Symposium (IMS) San Francisco, CA, USA, 22-MAY-16 - 27-MAY-16

32. Mooney J. et al, "Dithered Multi-Bit Sigma-Delta Modulator Based DPWM for DC-DC Converters", IEEE Applied Power Electronics Conference APEC, March 2015
 33. Halton M. et al, "Robust Analysis and Synthesis Design Tools for Digitally Controlled Power Converters", IEEE Applied Power Electronics Conference APEC, March 2015
 34. Pepe D. et al, "A 78.8-92.8 GHz 4-bit 0-360° Active Phase Shifter in 28nm FDSOI CMOS with 2.3 dB Average Peak Gain", Accepted for publication at IEEE European Solid State Circuits Conference (ESSCIRC), 2015
 35. Effler S., et al, "Scalable Digital Power Controller with Phase Alignment and Frequency Synchronization", IEEE Transactions on Circuits and Systems I (TCAS-I), 2014
 36. Ossieur P., et al, "A 1V 2mW 17GHz Multi-Modulus Frequency Divider Based on TSPC Logic Using 65nm CMOS", IEEE European Solid State Circuits Conference (ESSCIRC), 2014
 37. Kennedy M., et al., "0.3-4.3 GHz Frequency-Accurate Fractional-N Frequency Synthesizer with Integrated VCO and Nested Mixed-Radix Digital Delta-Sigma Modulator-Based Divider Controller", IEEE Journal of Solid State Circuits (JSSC), May 2014
 38. Ossieur P., et al, "A 10Gb/s Linear Burst-Mode Receiver in 0.25um SiGe:C BiCMOS", IEEE Journal of Solid State Circuits (JSSC), Feb 2013
 39. Mooney J., et al, "Application-Specific Instruction-Set Processor for Control of Multi-Rail DC-DC Converter Systems", IEEE Transactions on Circuits and Systems I (TCAS-I), January 2013
 40. Kennedy M., et al., "High Speed, High Accuracy Fractional-N Frequency Synthesizer using Nested Mixed-Radix Digital Sigma-Delta Modulators", IEEE European Solid State Circuits Conference (ESSCIRC), Sep 2013
 41. Scharrer M., et al, "Efficient Bi-directional Digital Communication Scheme for Isolated Switch Mode Power Converters", IEEE Transactions on Circuits and Systems I (TCAS-I), December 2012
- ### Other Publications
42. K. Pomorski, P. Giounanlis, E. Blokhina, D. Leipold, and R. B. Staszewski, "Analytic view on coupled single-electron lines", IOP Science – Semiconductor Science and Technology, 2019
 43. P. Giounanlis, E. Blokhina, D. Leipold, and R. B. Staszewski, "A Python-Verilog toolbox for modeling of a Hadamard gate based on position-based CMOS qubits," (ICECS), Nov. 2019
 44. V. Govindaraj, J. Du, Y. Hu, T. Siriburanon and R. B. Staszewski, "DTC-assisted all-digital phase-locked loop exploiting hybrid time/voltage phase digitization," (APCCAS), Nov. 2019
 45. Pourmousavian N, Siriburanon T, Feng-Wei Kuo, Babaie M, Staszewski RB, "Clock generation", chapter in Digitally Enhanced Mixed Signal Systems, pg 255-288, 2019
 46. K. Pomorski, P. Giounanlis, E. Blokhina, D. Leipold, and R. Staszewski, "Description of interface between semiconductor and superconducting quantum computer," XIX National Conference on Superconductivity, Oct. 2019
 47. G. Nikandish, R. B. Staszewski, and A. Zhu, "Breaking bandwidth limit: A review of broadband Doherty power amplifier design for 5G," IEEE Microwave Magazine, 2019.

48. G. Nikandish, R. B. Staszewski, and A. Zhu, "A broadband continuous class-F GaN MMIC PA using multi-resonance matching network," (EuMW) Sept. 2019
49. Y. Donnelly, M. P. Kennedy, J. Breslin, S. Tulisi, S. Patil, C. Curtin, S. Brookes, B. Shelly, P. Griffin, M. Keaveney, "4.48-GHz Fractional- N Frequency Synthesizer With Spurious-Tone Suppression via Probability Mass Redistribution", (SSC-L), Sep 2019
50. G. Nikandish, R. B. Staszewski, and A. Zhu, "Bandwidth enhancement of GaN MMIC Doherty power amplifiers using broadband transformer-based load modulation network," IEEE Access, 2019
51. G. Nikandish, R. B. Staszewski, and A. Zhu, "Broadband fully integrated GaN power amplifier with embedded minimum inductor bandpass filter and AM-PM compensation," (SSC-L), Sept. 2019
52. V. Mazzaro, M. P. Kennedy, "Another moving Spur Phenomenon observed in a MASH-based Fractional-N PLL", ISSC, June 2019
53. D. Mai, X. Li, M. P. Kennedy, "Experimental Confirmation of Wandering Spurs in a Commercial Fractional-N Frequency Synthesizer with a MASH 1-1-1 Divider Controller", ISSC, June 2019
54. Z. Gao, Y. Hu, T. Siriburanon, and R. B. Staszewski, "28GHz quadrature frequency generation exploiting injection locked harmonic extractors for 5G communications," (NEWCAS), June. 2019
55. E. Koskin, P. Bisiaux, D. Galayko, E. Blokhina, "All-Digital Phase-Locked Loop Arrays: Investigation of Synchronisation and Jitter Performance through FPGA Prototyping", (NEWCAS), June 2019
56. Y. Hu, T. Siriburanon, and R. B. Staszewski, "Intuitive understanding of flicker noise reduction via narrowing of conduction angle in voltage-biased oscillators", (TCAS-II), 2019
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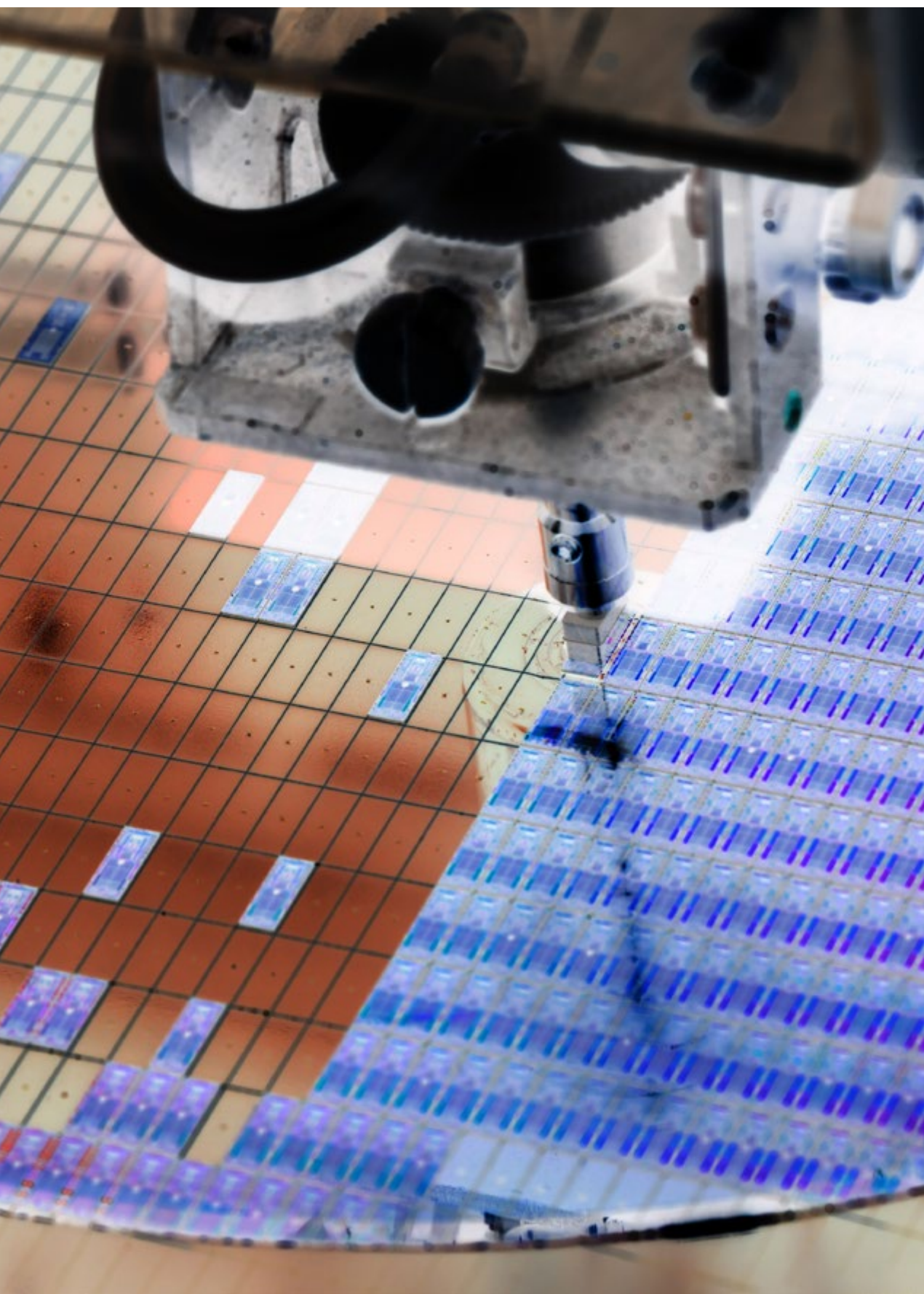
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