15 bit, 2nd Order Noise Shaped SAR @ 1MS/sec

Abstract:

Since the introduction of 90nm CMOS Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However the best performing ADCs from a power consumption point of view have 10bits of resolution and a signal bandwidth of <1MHz. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic which all benefit from faster CMOS technologies. This work aims to leverage this speed advantage through oversampling and noise shaping to achieve an ADC with greater precision.

Introduction

The most efficient ADCs are limited by thermal noise. The comparator adds thermal noise and the faster the SAR ADC the larger the comparator noise bandwidth and its total integrated noise. The first Panther ADC chip consisted of a 10 bit SAR core, a noise shaping loop filter use duty cycled open loop trans-conductance (GM) stages as integrators and a summing comparator. The performance of this ADC was limited by the wideband thermal noise of the GM stages and the fact that the integrators were designed for a fixed clock frequency.

Target Specifications:

Specification Name	Typical	Description
Sampling rate	75MS/s	rate at which input signal is sample 2ns S&H time
SAR clock rate (synchronous)	1.5GS/s	Synchronous timing uses an external clock
Resolution w/o shaping	10ENOB	resolution of SAR core 10bits + 2 redundant bits
Input signal bandwidth	1MHz	target signal frequency
Resolution with shaping	15ENOB	Target resolution for shaped ADC
SNDR @100kHz	90dB	Target resolution for signals at 1MHz
Supply voltage	0.9V	Use core supply if possible to reduce number of supply pins
Power	<5 mW	Power to create a competitive FoM

ADC Architecture and Model:

For the Panther2 ADC an error feedback topology had been implemented, Fig. 1. The error feedback topology samples the residue at the end of one conversion and creates a gained version of the residue on a capacitor. This gained residue is capacitively subtracted from the next sampled value of the ADC input. A first order feedback filter has been used as this has the lowest circuit thermal noise. The residue sample and gain circuit uses a dynamic amplifier gain stage which allows the loop filter thermal noise and power consumption to be reduced. Self-timing is added to the dynamic amplifiers to allow the loop filter to operate independently to the ADC rate.

For Panther 3 A new MASH topology has been proposed. We believe this topology is less susceptible to thermal noise in the noise shaping loop than previously published topologies. The 2nd order shaping allows the core SAR resolution to be reduced to 6 bits. Fig.2 shows a diagram illustrating the operation of the topology. Residue voltages are stored at different times in the conversion cycle and then added back to the main capacitor bank. The digital code from the second conversion is differentiated to high pass filter its errors and noise.

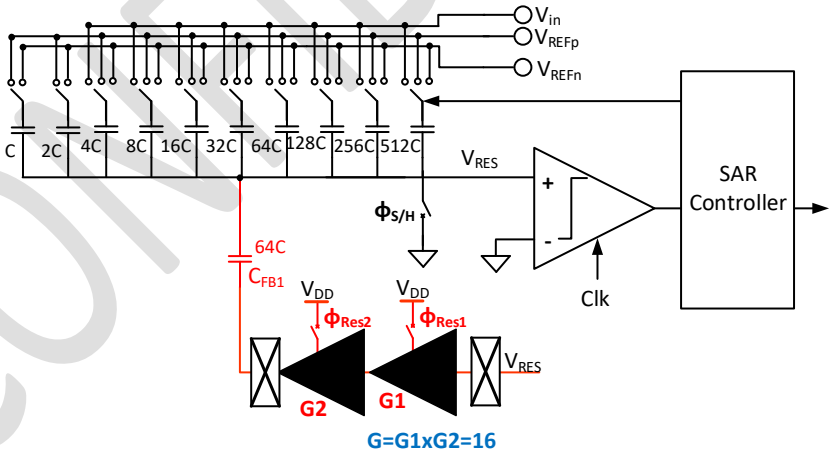

Figure 1: panther2v3 noise shaping path

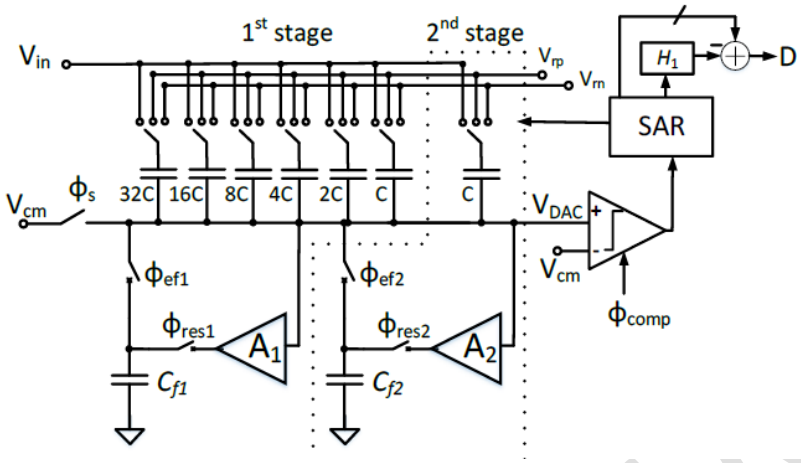

Figure 2: Panther 2V3 topology

Panther2v3 update:

Further testing on the FIBBED panther 2v3 parts was carried out, achieving improved SNDR results. It has been discovered that SNDR limitations partially came from the used Keysight 33500B signal generator, which was producing a spurious tone at around 180kHz. This was fixed by using a higher precision signal generator, the SR1, which helped to boost the SNDR to 78dB. This is illustrated in Figs. 3.

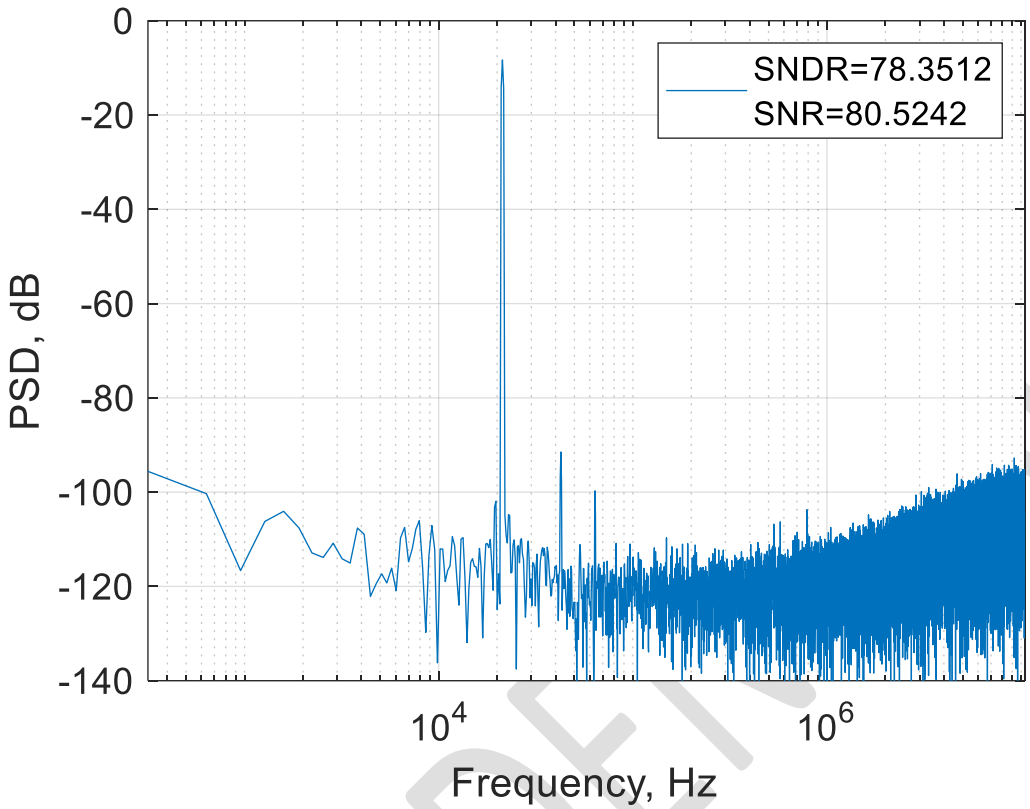

Figure 5: Panther 2v3 FIBBED part SNDR results using the SR1 signal generator

Panther3 update:

A paper was submitted to the IEEE VLSI conference on the 7th / Feb / 2022, a screenshot of the first page of the paper is presented below. Unfortunately, on the 31st / 03 /2022 we were notified that the submitted paper was not accepted for publication. The IEEE VLSI conference does not provide feedback for authors; it only produces a binary decision.

A 77 dB SNDR 1-1 MASH Noise Shaping 6 bit SAR

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Abstract

This paper presents the first MASH 1-1 error feedback noise shaping topology implemented in a single Noise Shaping SAR, which eliminates the need for inter-stage gain. The inclusion of an additional noise shaping stage, which leverages the unused 1C capacitor within the CDAC, further extends the capability of the noise shaping SAR architecture. The design is implemented in 28 nm CMOS and achieves an SNDR of 77 dB from a 6 bit CDAC.

Keywords: MASH, SAR, ADC, CMOS, noise-shaping, error-feedback.

Introduction

The achievable resolution of a SAR ADC, which is limited by the number of bit trails, can be extended through the introduction of oversampling and noise shaping (NS). The Error Feedback (EF) NS-SAR efficiently implements noise shaping by adding the SAR residue voltage to the next input [1-2]. However, the works in [2-3] highlighted that the two main design challenges associated with high-order loop filters in EF NS-SARs are the increased noise and coefficients' sensitivity. In [3], a 4th order cascaded NS-SAR was proposed, implementing two 2nd order loop-filters, reducing the filter coefficients' sensitivity and noise compared to a single loop 4th order filter implementation, at the cost of a bridge capacitor introduced within the SAR CDAC. This work proposes a 1-1 MASH SAR, where both first order stages are implemented using an unmodified single SAR CDAC. Hence there is no requirement for any gain stage between the 1st and 2nd stages. Instead, both stages co-exist within a single CDAC.

Proposed 1-1 MASH NS-SAR

Fig. 1 shows the signal-flow diagram of the proposed 1-1 MASH structure consisting of two EF stages. Both EF stages are shown separately for simplicity, however, in practice both stages utilize the same comparator and CDAC. The 1st stage operates as a standard EF NS SAR, whereby after N bit trials, the residue voltage, $V_{res1}(n)$, is sampled and stored prior to sampling the next input signal. However, prior to sampling the next input signal an additional operation is performed. The previously sampled residue voltage from the 2nd stage, $V_{res2}(n-1)$, is now added to $V_{res1}(n)$, and an additional bit-trail is completed resulting in the single bit output code, D_2, as described in Fig.1. D_2, the output from the single comparator decision is then passed through the digital cancellation logic, H_1, in order to cancel out V_{res1} and realize a 2nd order Noise-Transfer-Function (NTF).

Circuit implementation

The corresponding schematic is shown in Fig. 2, which consists of a 6-bit CDAC and two additional feedback capacitors C_{f1} and C_{f2}, which are used to sample and store V_{res1} and V_{res2}, respectively. The timing diagram in Fig. 2 highlights the operation of the proposed MASH topology, whereby the input signal is sampled onto the CDAC as normal. After which the $V_{res1}(n-1)$ from the previous conversion is added to the input using C_{f1}. The SAR logic then performs the 6 bit-trials upon completion of which the new residue voltage, $V_{res1}(n)$, is amplified by the gain stage A_1 and stored on C_{f1}. Then the residue voltage, $V_{res2}(n-1)$, is

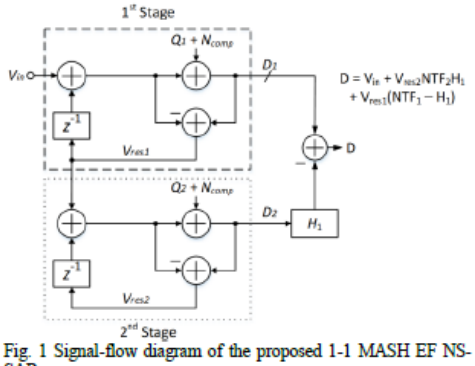

Fig. 1 Signal-flow diagram of the proposed 1-1 MASH EF NS-SAR.

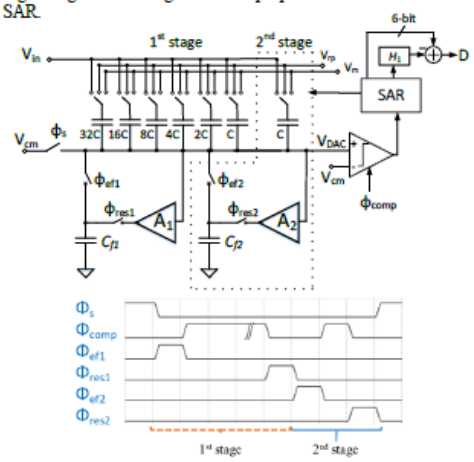

Fig. 2 Simplified schematic of the proposed 1-1 MASH prototype.

added to the CDAC where one additional bit-trial is completed leveraging the additional 1C attenuation capacitor. The new resultant residue voltage, $V_{res2}(n)$, is then amplified and stored on C_{f2}. As the sampled input signal remains on the CDAC throughout the conversion, there is no inter-stage gain. By eliminating the requirement for any gain stage between the two stages, it significantly simplifies the requirements of H_1 as there is no inter-stage gain mismatch to contend with.

Both A_1 and A_2 gain stages are realized using a 2-stage Dynamic Amplifier (DA) as shown in Fig. 3. The 2-stage approach is adopted to reduce the input referred noise, and improve linearity, while simultaneously relaxing the gain requirements of each DA stage. With both stages having a nominal gain of 4, resulting in a combined gain of 16, this ensures that C_{f1} and C_{f2} are only 4C.

Measurement results

The proposed ADC was implemented in a 28nm CMOS process with an active silicon area of 0.094mm^2. The chip-micrograph is shown in Fig.4, showing the solder bumps associated with the Chip-Scale-Packaging. The single-ended total CDAC is 3.8pF. The chip consumes 0.990mW from a

Figure 4: Panther 3 paper screenshot submitted to IEEE VLSI.

Summary

Panther 2V3: Further testing on FIBBED part was carried out finding a source of distortion coming from Keysight 33500B generator, the best up to date performance is now 78dB SNDR using the SR1 generator.

Panther 3 paper was submitted to IEEE VLSI but, unfortunately, it was not accepted for publication.

Next Steps:

- Panther 2V3: Try to further improve SNDR results and write a paper for an IEEE journal.
- Panther 3: Contact well recognized researchers in the area, from whom we can obtained valuable feedback for the re-writing of the paper. Use the feedback to preparing the paper the paper resubmission, this time for IEEE Journal of Slid State Circuits (JSSC) or the IEEE TCASI.