# 15 bit, 2nd Order Noise Shaped SAR @ 1MS/sec


## Abstract:

Since the introduction of 90nm CMOS Successive Approximation Register (SAR) ADCs have become the dominant low power ADC architecture. However the best performing ADCs from a power consumption point of view have 10bits of resolution and a signal bandwidth of <1MHz. The key blocks in SAR ADCs are capacitors, comparators, timing logic and processing logic which all benefit from faster CMOS technologies. This work aims to leverage this speed advantage through oversampling and noise shaping to achieve an ADC with greater precision.


## Introduction

The most efficient ADCs are limited by thermal noise. The comparator adds thermal noise and the faster the SAR ADC the larger the comparator noise bandwidth and its total integrated noise. The first Panther ADC chip consisted of a 10 bit SAR core, a noise shaping loop filter use duty cycled open loop trans-conductance (GM) stages as integrators and a summing comparator. The performance of this ADC was limited by the wideband thermal noise of the GM stages and the fact that the integrators were designed for a fixed clock frequency.

## Target Specifications:

| Specification Name | Typical | Description |
|---|---|---|
| Sampling rate | 75MS/s | rate at which input signal is sample 2ns S&H time |
| SAR clock rate (synchronous) | 1.5GS/s | Synchronous timing uses an external clock |
| Resolution w/o shaping | 10ENOB | resolution of SAR core 10bits + 2 redundant bits |
| Input signal bandwidth | 1MHz | target signal frequency |
| Resolution with shaping | 15ENOB | Target resolution for shaped ADC |
| SNDR @100kHz | 90dB | Target resolution for signals at 1MHz |
| Supply voltage | 0.9V | Use core supply if possible to reduce number of supply pins |
| Power | <5 mW | Power to create a competitive FoM |

**ADC Architecture and Model:**

For the Panther2 ADC an error feedback topology had been implemented. The error feedback topology samples the residue at the end of one conversion and creates a gained version of the residue on a capacitor. This gained residue is capacitively subtracted from the next sampled value of the ADC input. A first order feedback filter has been used as this has the lowest circuit thermal noise. The residue sample and gain circuit uses a dynamic amplifier gain stage which allows the loop filter thermal noise and power consumption to be reduced. Self-timing is added to the dynamic amplifiers to allow the loop filter to operate independently to the ADC rate.

**Panther2v3 testing:**

Panther2 revision 3 Silicon is in our lab. The core SAR behaves well but unfortunately the dynamic amplifier in the noise shaping look is not working. To debug we have used the register controlled trim bits and analysed the current consumption of the Dynamic amplifier. We have also tested turning on and off the chopping mode and adding dc offsets to the first amplifier stage. On the parts we have tested none of these tests have allowed us to see the dynamic amplifier functioning the way we expect.

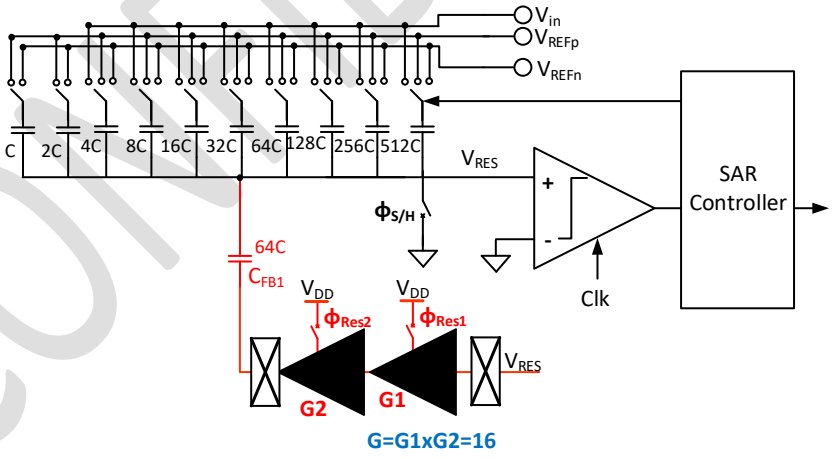


*Figure 1: panther2v3 noise shaping path*

**Panther3 a new noise shaping topology:**

A new MASH topology has been proposed. We believe this topology is less susceptible to thermal noise in the noise shaping loop than previously published topologies. The 2nd order shaping allows the core SAR resolution to be reduced to 6 bits. Fig.2 shows a diagram illustrating the operation of the topology. Residue voltages are stored at different times in the conversion cycle and then added back to the main capacitor bank. The digital code from the second conversion is differentiated to high pass filter its errors and noise. FFT plots of the ADC schematic and extracted simulation responses are shown in Fig. 3 and Fig. 4.

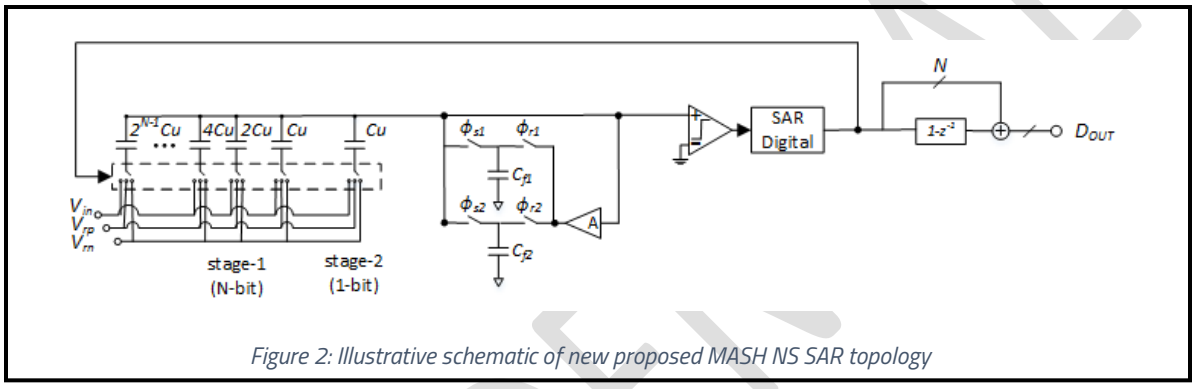


*Figure 2: Illustrative schematic of new proposed MASH NS SAR topology*

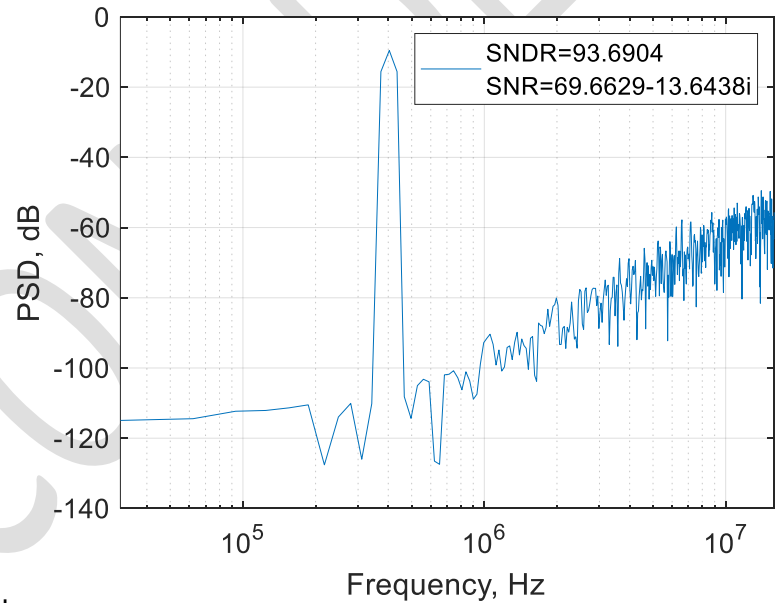


*Figure 3: Schematic results for panther3*

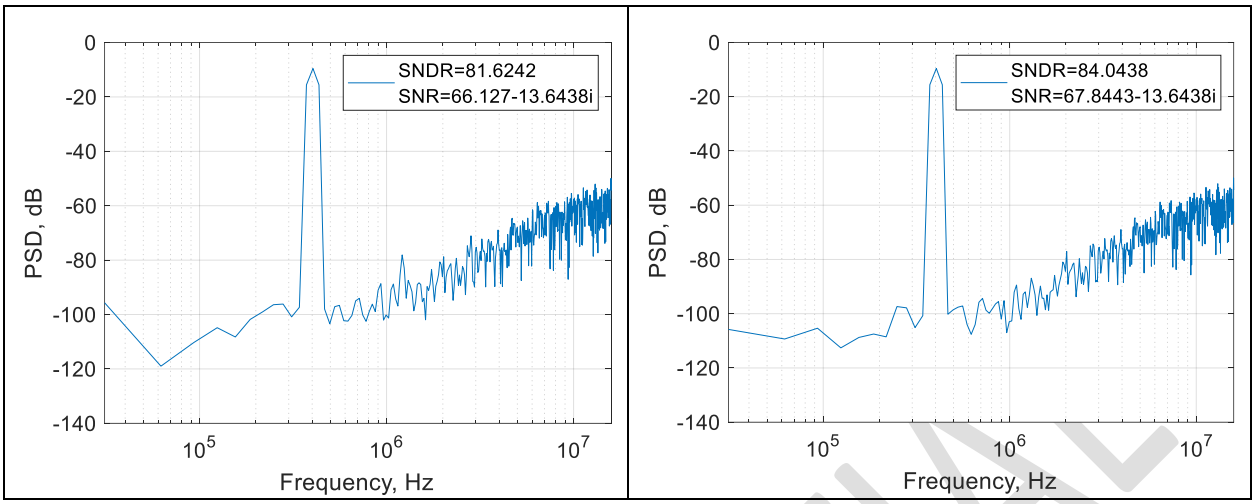


*Figure 4: Simulated results of Analog core extracted (without calibration left and calibrated right)*

**Panther2v3 update:**

MASER engineering delivered the FIBBED panther 2v3 parts. The first part tested showed working noise shaping, validating the fix, results from this part are shown in Figure 5. The shows a calibrated 10bit SAR with and without noise shaping. The initial results in Figure 5 show an improvement from 69.8dB to 75dB. By optimizing the gain parameters in the dynamic amplifier an enabling the amplifier chopping further SNR improvements can be achieved.

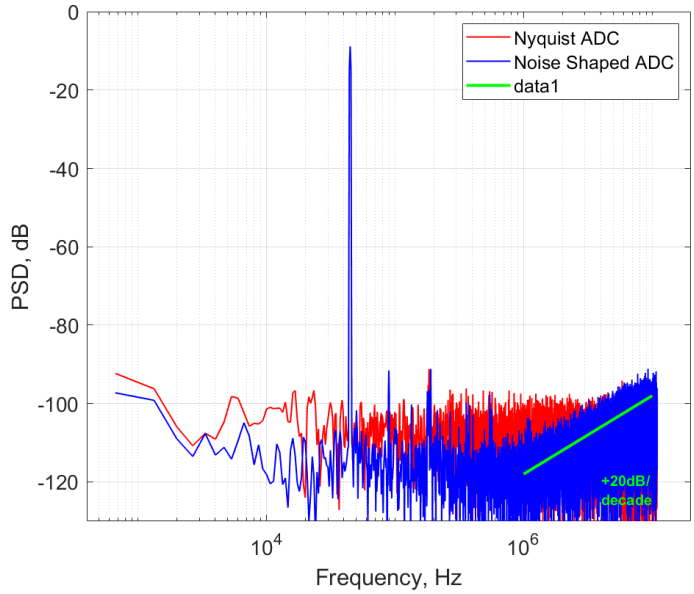


*Figure 5: Panther 2v3 measurements on a Fibbed chip showing SNR with and without noise shaping. SNR improves from 69.8dB to 75dB when NS is turned on*

**Panther3 update:**

Panther 3 proposes a 2nd order noise shaping SAR that that uses a 6-bit core SAR and two independent 1st order feedback loops. The resulting topology is more robust to feedback's coefficient variations than the conventional 2nd order topologies. Panther 3 silicon was tested, showing a clear 40dB/dec slope with SNDR and SNR of 74.5dB and 77dB, respectively, as it illustrated in Fig. 5 (a). These results are less than 10dB below the schematic simulations, also depicted in Fig. 5(b), which did not include parasitic CDAC extraction due to the unfeasible simulation time demands. Resolution wise, panther 3 silicon shows state of the art performance, comparable to works published in 2020 and 2021, and we have plans to submit a paper to VLSI and/or JISSCC in early 2022.

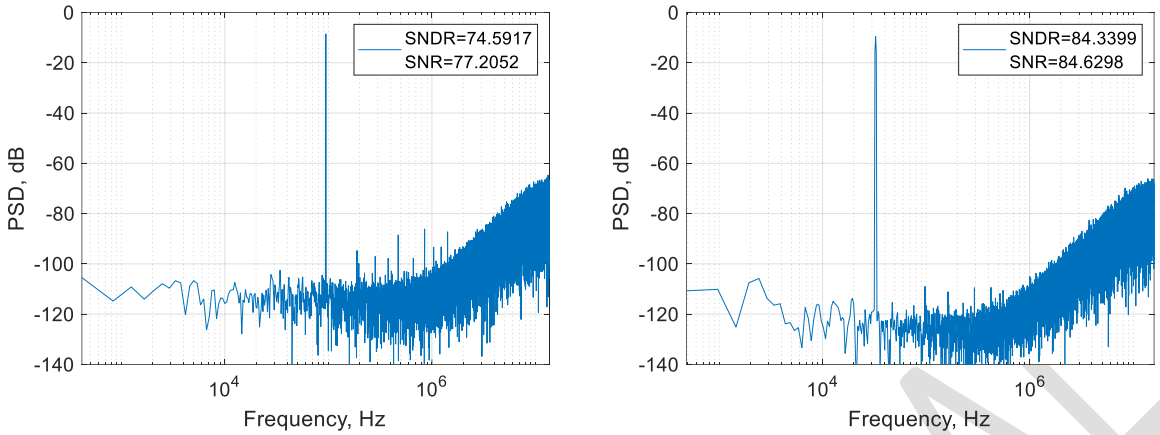


*Figure 6: Panther 3: 2nd order noise shaping with a 6-bit core SAR and two independent 1st order feedback loops, (a) Silicon results and (b) simulation results.*

## Panther 4

Not happening, it was decided that panther 3 was the last panther tape-out.

## Summary

Panther 3 silicon results showed state of the art results of SNDR and SNR of 74.5dB and 77dB with only a 6-bit core SAR and a novel 2nd order noise shaping implementation. A paper with this results will follow.

## Next Steps:

- Test Panther 3 paper writing and submission.