# Novel Modulators for Low-Spur BB-PLLs

**Abstract**

This project is in two parts: (i) development of a modulator controller that, when incorporated in a fractional-N BB-PLL, produces lower spurs and noise than a MASH-based controller and (ii) development of a DCO controller that produces lower noise and spurs than a conventional MASH-based controller. This report summarizes progress over the past twelve months.

**Introduction**

BB-PLLs are cheap and easy to implement but suffer from a range of problems associated with nonlinear components. Apart from noise due to physical components, there are at least four sources of quantization noise: the bang-bang phase detector, the DCO and, in the case of a fractional-N frequency synthesis, the modulator and DTC that implement fractional division.

Quantization noise is fundamentally mathematical in nature. We will use mathematics to mitigate/eliminate it. The core technique we will exploit is PMR, which we demonstrated in a CP-PLL and set a new record at ISSCC 2019 for measured worst-case inband fractional spurs. KAIST presented a variant of PMR at ISSCC 2020 that set a new record for worst-case inband fractional spurs in an ADPLL with a ring DCO.

Fractional-N BB-PLLs still lag significantly behind CP-PLLs in terms of their spur performance. This work will help us to close the gap.

The project is in two parts: (i) development of a modulator controller that, when incorporated in a fractional-N BB-PLL, produces lower spurs and noise than a MASH-based controller and (ii) development of a DCO controller that produces lower noise and spurs than a conventional MASH-based controller.

Luca Avallone and Xu Wang were addressing the modulator that enables fractional-N division and interacts with the bang-bang nonlinearity. High-level models of the BB-PLL were being designed and validated at system level. Luca Avallone graduated after publishing the integer-N model and Xu Wang discontinued his studies in December 2021; the fractional-N part has been on hold since then.

Valerio Mazzaro has been working on the DCO and its modulator. He has developed, simulated and filed a patent application for a novel spur-free divider controller architecture for the DCO. Valerio Mazzaro took up full-time employment in May 2022. ME student Conor Kneafsey is working on the FPGA implementation.

**Part I: Feedback Divider Controller (Luca Avallone, Xu Wang, Peter Kennedy)**

**State of the Art**

Until 2021, the best model of an integer-N bang-bang PLL in the literature was that due to Xu and Abidi [1]. We developed a high-level theoretical model that accurately predicts the simulated performance [2]. Similar predictions for the fractional-N mode do not yet exist.

**Next Steps**

With an anticipated no-cost extension, we plan to model fractional-N behaviour by adding a multimodulus divider, DTC, and divider controller in the feedback path of our integer-N model. We will validate the phase-domain model with a conventional MASH 1-1 divider controller and then compare the fractional-N performance with that of a PMR-based divider controller.

**Part II: DCO Controller (Valerio Mazzaro, Conor Kneafsey, Peter Kennedy)**

**State of the Art**

To achieve high frequency resolution, a DCO is driven by a noise-shaping modulator, typically a MASH 1-1. When the shaped quantization noise of the modulator interacts with the nonlinearity of the capacitive DAC, excess spurs and folded noise are produced. The state of the art is to use *dither* to mitigate idle tones and *dynamic element matching* (DEM) to mitigate nonlinearity-induced spurs; both techniques introduce additional noise. We are using a different type of noise-shaping modulator that hopefully will both eliminate the spurs and introduce less pink noise.

**Results to Date**

The reference model in the literature is due to Zhuang *et al*. [3]. This considers a DCO with a dithered MASH 1-1 controller (to increase resolution) and DEM (to mitigate nonlinearity-induced noise and spurs). Fig. 1 shows the simulated phase noise with (a) conventional and (b) novel divider controllers; the latter has lower low frequency noise.

The novel family of divider controllers is provably spur-free when used in conjunction with a memoryless nonlinearity. We have filed a provisional patent on this divider controller family [4].

**Next Steps**

We will validate the phase noise predictions of Fig. 1 by implementing the divider controllers on an FPGA and using a high-resolution DAC to emulate capacitor mismatch in a DCO.

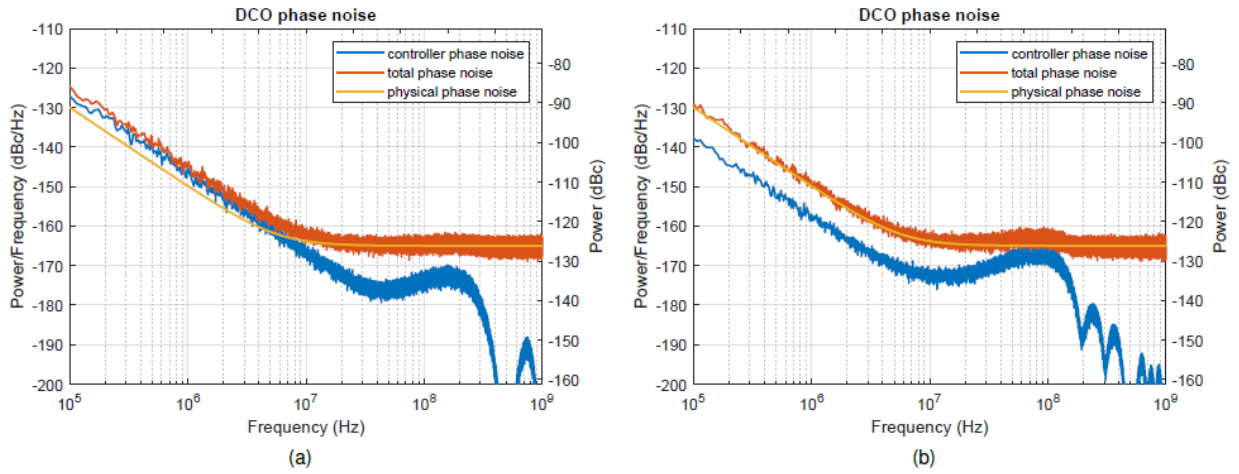


Fig. 1. Phase noise of mismatched low noise DCO with (a) conventional and (b) novel controllers.

## Summary

The integer-N BB-PLL model has been validated. Next, we will extend it to the fractional-N case, incorporate the PMR-based divider controller and compare the MASH and PMR solutions.

The novel DCO controller has the potential to outperform a MASH controller in the case of low-noise DCOs. Next, we will validate the performance by means of an FPGA-DAC-based emulator.

## References

[1] H. Xu and A. A. Abidi, "Design Methodology for Phase-Locked Loops Using Binary (Bang-Bang) Phase Detectors," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 7, pp. 1637-1650, July 2017, doi: 10.1109/TCSI.2017.2679683.

[2] L. Avallone, M. Mercandelli, A. Santiccioli, M. P. Kennedy, S. Levantino and C. Samori, "A Comprehensive Phase Noise Analysis of Bang-Bang Digital PLLs," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 7, pp. 2775-2786, July 2021, doi: 10.1109/TCSI.2021.3072344.

[3] J. Zhuang, K. Waheed and R. B. Staszewski, "Design of Spur-Free ΣΔ Frequency Tuning Interface for Digitally Controlled Oscillators," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 1, pp. 46-50, Jan. 2015, doi: 10.1109/TCSII.2014.2362692.

[4] V. Mazzaro and M.P. Kennedy. “Digital delta sigma modulator with inherent spur immunity after nonlinear distortion,” U.S. Patent application, 11 April 2022.