Charge-Sharing Locking Fractional-*N* Frequency Synthesis

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Abstract:

Ultra-low jitter (sub-100fs/50fs) frequency synthesis is highly desirable for 5G/6G RF and mm-Wave (mmW) communications to support the complex modulation schemes (e.g., 1024QAM). The idea of charge-sharing locking is that the capacitor of the *LC* tank itself will be periodically charge-shared with another capacitor charged by a DAC to a voltage that is expected from a waveform at that particular time point, resulting in an instantaneous phase correction. The resulting voltage change will be detected and used to correct the DCO frequency. This results in a great simplification of circuitry and consumed power while delivering sub-100fs integrated jitter.

1. Proposed CSL architecture:

Figure 1 shows the basic concept of charge-sharing locking (CSL). At the heart lies the *LC*-tank oscillator generating a (near) sinusoidal waveform of frequency. During the high-level of reference clock *ref*, the digital logic (DIG) driving the DAC presets V_{share} on the sharing capacitor C_{share} (via switch S_1) to the expected oscillator waveform voltage at the significant reference instances (defined as *ref*'s falling edges. Afterwards, a narrow pulse shortly connects C_{share} to C_{osc} (i.e., S_1 OFF, S_2 ON) for the actual CSL operation. After the charge-sharing operation with the oscillator is completed, the charge residue leftover in the C_{share} will contain information of the frequency deviation. This voltage is digitized by a SAR-ADC upon asserting *clk_q_trans*. The ADC output is passed through the DZ, accumulator, and attenuation factor KI (affecting the convergence speed) to generate the oscillator tuning word (OTW).
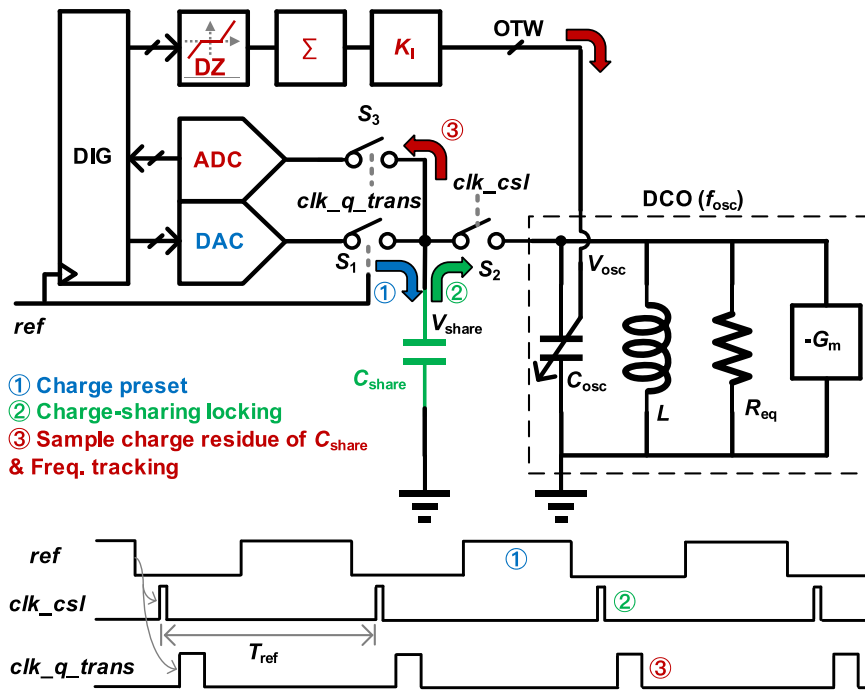
Fig .1. Basic architecture of charge-sharing locking.

2. Proposed Digital-to-Time Converter

To support fractional-N operation in CSL, a high-performance digital-to-time converter based on RC-delay is introduced. Several techniques are employed to mitigate the nonlinearity of DTC, including linearized R and C, dummy cap-bank for stabilizing the supply ringing, etc. The post simulated performance of DTC is shown in Fig. 2, achieving 9-bits, LSB: ~500 fs, INL: < 0.3 LSB, power < 0.5 mW.
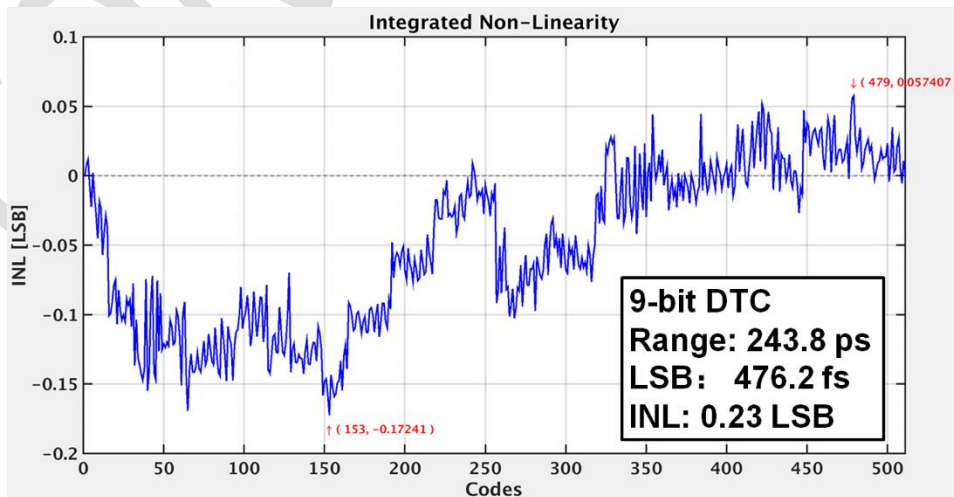

Fig .2. Post simulation of the proposed digital-to-time converter (DTC) supporting fractional-N CSL.

3. Simulation Results

Due to the complexity of mixed-signal (including RF) system of CSL-PLL, it is almost impossible to run "full" post-simulation with the whole chip. Instead, we model some relative individual blocks, e.g., ADC, DAC, DTC, with Verilog-AMS models, matching their own post-simulation results with their Verilog-AMS models. The whole chip simulation is running with Verilog-AMS models, Calibre View and EMX S-parameters (for DCO).

Fig. 3 shows the post-simulated rms jitter and spur performance. It achieves sub-30 fs and sub-50 fs rms jitter for integer-N and fractional-N operation. Due the high-linearity of the proposed DTC, the in-band spur is around -59 dBc. To the best of authors' knowledge, this is the best performance for fractional-*N* PLL, demonstrating the advantage of CSL.
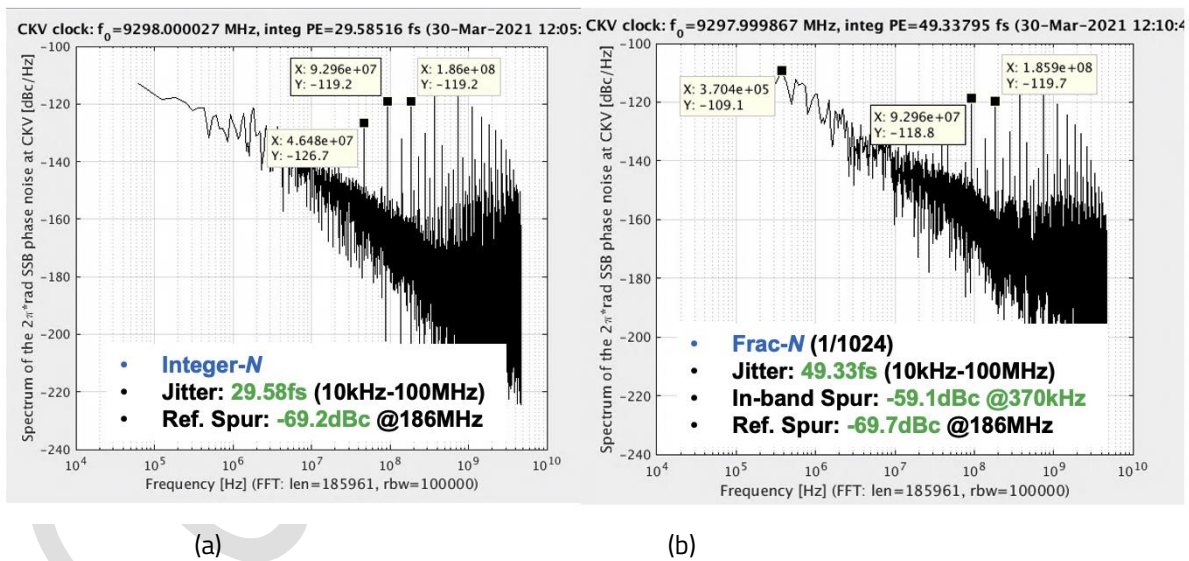

Fig. 3 Simulated rms jitter and spur performance for CSL: (a) Integer-*N* operation (b) Fractional-*N* operation (fractional number = 1/1024).

4. Tape-out:

In May 2021, the chip (occupying 1.3mm * 1.4mm) was successfully tape-out, as shown in Fig. 4. Silicon was received in September.
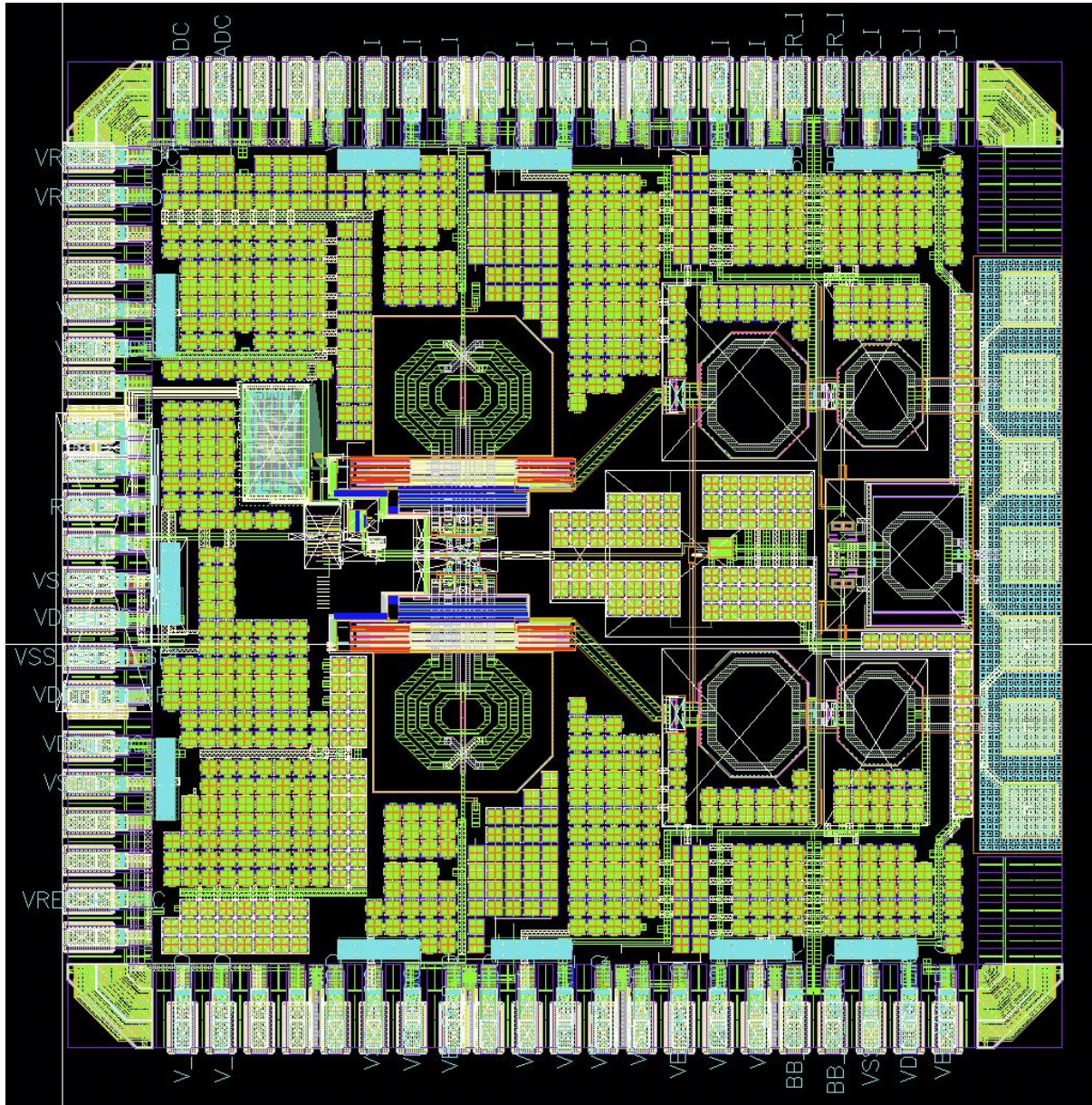
Fig. 4. Chip layout in TSMC 28nm LP (1.3mm * 1.4mm).

5. Measurement

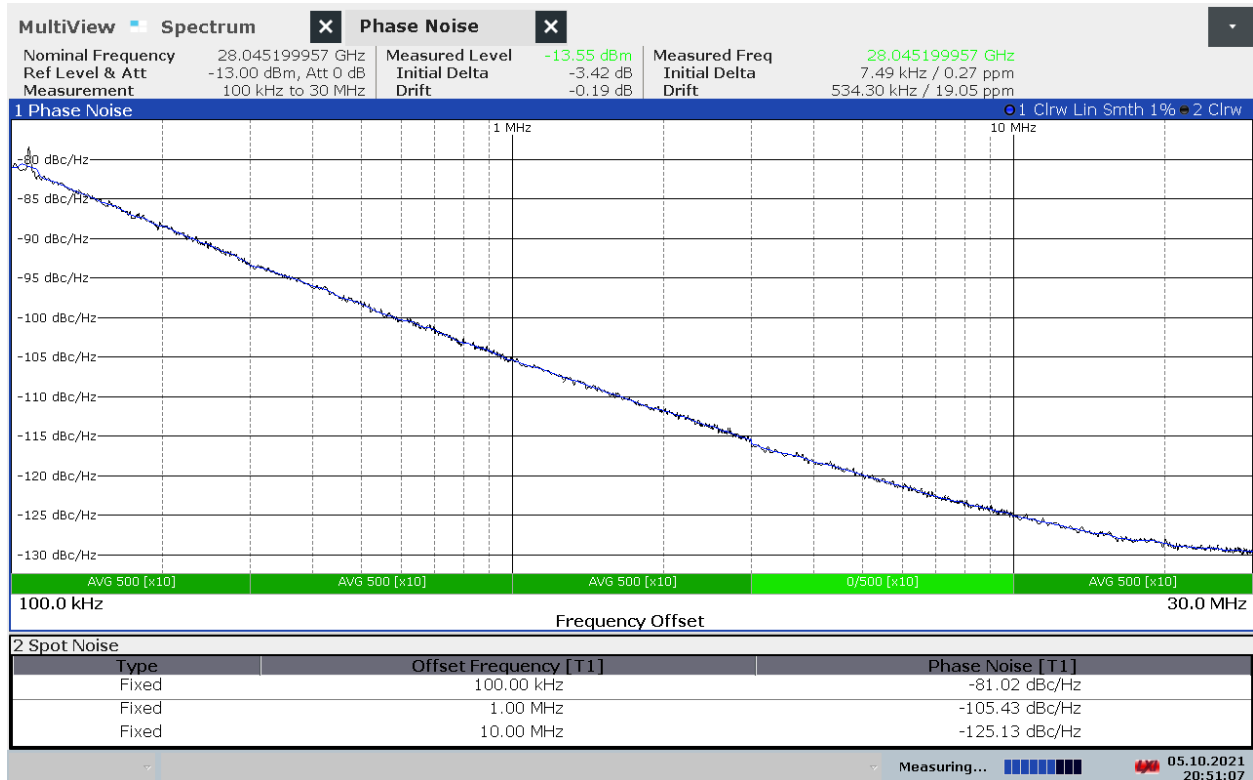### 1. 28GHz Quadrature DCO Free Running Testing:

Fig. 5. PN plot of 28GHz quadrature free-running oscillator.

The measured PN of the 28GHz quadrature DCO achieves phase noise @1MHz -105dBc/Hz with low flicker PN corner < 200kHz. Its PN@1MHz is more than 10dB better than other state-of-the-art quadrature oscillators in this frequency range.
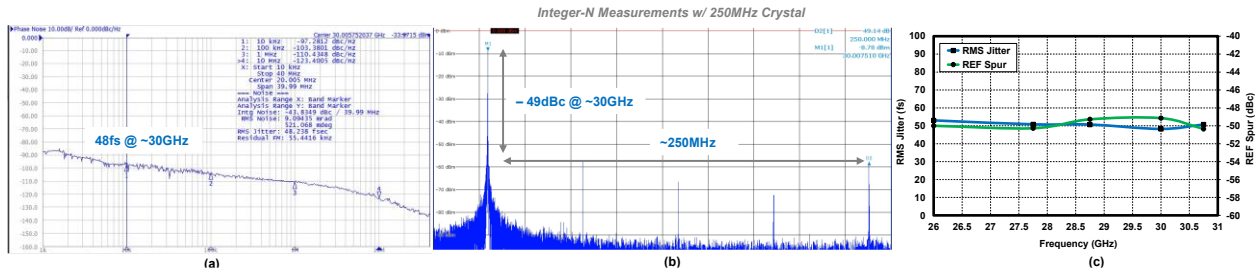
2. Close-loop Measurements

Fig. 6 Integer-N measurements with 250MHz crystal: (a) Phase noise, rms random jitter, and (b) reference spurs at 30GHz. (c) RMS random jitter and reference spurs over the tuning range.
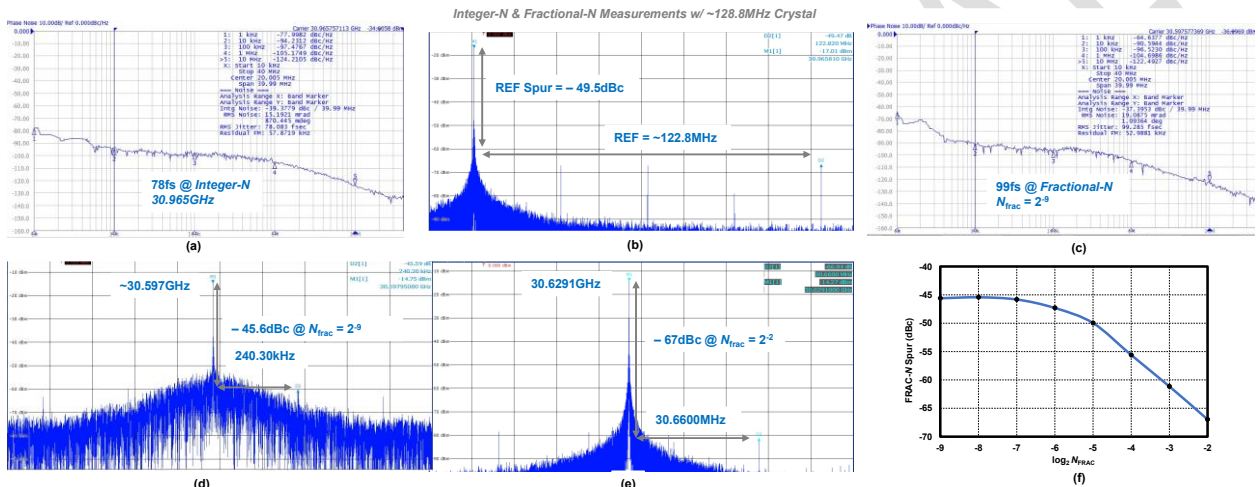

Fig. 7 Integer-N and fractional-N measurements with 128.8 MHz crystal: (a) Phase noise, rms random jitter, and (b) reference spurs at integer-N mode. (c)--(f) Phase noise, rms random jitter, and spurs at fractional-N mode.

6. Achievements

There are several papers (**1 JSSC, 1 TCAS-I, and 2 TCAS-II**) with this project have been published, explained in detail about the low jitter mechanisms of charge-sharing locking and low flicker phase noise DCO. The detailed list are as follows:

- **Y. Hu**, X. Chen, T Siriburanon, J. Du, V. Govindaraj, A. Zhu and **R. B. Staszewski**, "A charge-sharing locking technique with a general phase noise theory of injection locking", *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 57, iss. 2, pp. 518–534, Feb. 2022.

- **Y. Hu**, T. Siriburanon and **R. B. Staszewski**, "Multirate Timestamp Modeling for Ultra-Low-Jitter Frequency Synthesis: A Tutorial (Invited Paper)", *IEEE Trans. on Circuits and Systems II (TCAS-II)*, vol. 69, iss. x, pp. xx–xx, xx. 2022.

- **Y. Hu**, T. Siriburanon and **R. B. Staszewski**, "Oscillator flicker phase noise: A tutorial (Invited Paper)", *IEEE Trans. on Circuits and Systems II (TCAS-II)*, vol. 68, iss. 2 pp. 538–544, Feb. 2021.

- X. Chen, **Y. Hu***, T. Siriburanon, J. Du, **R. B. Staszewski,** and A. Zhu, "Flicker Phase Noise Reduction Using Gate–Drain Phase Shift in Transformer-Based Oscillators", IEEE Trans. on Circuits and Systems I (TCAS-I), vol. 69, iss. 3, pp. 973–984, Mar. 2022.

Besides, two JSSCs manuscripts are under writing about fractional-N CSL and ultra-low flicker phase noise quadrature DCO, which will be submitted soon.

Future work:
- JSSC writing