High bandwidth Voltage Controlled Oscillator based Analog to Digital Converters by interleaving techniques

Abstract:

This project will investigate the techniques to increase the bandwidth in Voltage Controlled Oscillator (VCO) based Analog-to-Digital Converters (ADCs) by interleaving. Unlike the regular interleaving ADCs, only the single core (VCO) of the ADC will be used and interleaving is applied to the Frequency to Digital Converter (FDC) which is mostly digital circuit and easily scalable with technology. This idea enables us to achieve the higher bandwidth (and speed) with the minimum cost is terms of power and area. Other side, the non-linearity of VCO Voltage to Frequency (V-to-F) tuning curve is the bottle neck to achieve the higher accuracy in VCO based ADCs. This will limit the performance of an ADC to 6-7bits. We are trying to incorporate the digital calibration techniques to improve the linearity along with the bandwidth.

Research challenge:

Following are the research challenges involved in this project:

1. Investigating the interleaving mechanisms to increase the bandwidth (and/or speed)
2. Investigating the mechanisms to reduce the quantisation noise by means of increasing the noise shaping order or by averaging.
3. Investigating the calibration mechanisms (on/off-chip with digital/analog) to improve the linearity.

Proposed plan:

We are proposing to develop a higher bandwidth VCO based ADC with focus on the following novelties:

1. First we propose to develop the single channel ADC with 12bits 100MS/s performance.

2. Then focus on non-linearity correction mechanisms (on/off-chip with/without digital calibration techniques).
3. Then we will introduce the interleaving by x8 channels.
4. Multiple tape-outs are planned in order to develop this.
5. Targeted for tier-I conference publications such as ISSCC, VLSI Symposium, CICC, ESSCIRC and journal publications such as JSSC, SSC-I, TCAS-I.

Current status:

First version of system model design is under progress and we plan to migrate this to partial schematic and Verilog-A model simulation as a next step.