Novel Modulators for Low-Spur BB-PLLs

Abstract

This project is in two parts: (i) development of a modulator controller that, when incorporated in a fractional-N BB-PLL, produces lower spurs and noise than a MASH-based controller and (ii) development of a DCO controller that produces lower noise and spurs than a conventional MASH-based controller. This report summarizes progress to date on model development and analysis.

Introduction

BB-PLLs are cheap and easy to implement but suffer from a range of problems associated with nonlinear components. Apart from noise due to physical components, there are at least four sources of quantization noise: the bang-bang phase detector, the DCO and, in the case of a fractional-N frequency synthesis, the modulator and DTC that implement fractional division.

Quantization noise is fundamentally mathematical in nature. We will use mathematics to mitigate/eliminate it. The core technique we will exploit is PMR, which we demonstrated in a CP-PLL and set a new record at ISSCC 2019 for measured worst-case inband fractional spurs. KAIST presented variants of PMR at ISSCC 2020 which set a new record for worst-case inband fractional spurs in an ADPLL with a ring DCO.

Fractional-N BB-PLLs still lag significantly behind CP-PLLs in terms of spur performance. This work will help us to close the gap.

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(ii) development of a DCO controller that produces lower noise and spurs than a conventional MASH-based controller.

Luca Avallone and Xu Wang have been addressing the modulator that enables fractional-N division and interacts with the bang-bang nonlinearity; Valerio Mazzaro is focussing on the DCO and its modulator. High-level models of the fractional-N BB-PLL are being designed and validated at system level. Possible divider controller architectures for the DCO have been evaluated.

Part I: Feedback Divider Controller (Luca Avallone, Xu Wang, Peter Kennedy)

State of the Art

Until this year, the best model of an integer-N bang-bang PLL in the literature was that due to Xu and Abidi [1]. We developed a high-level theoretical model that accurately predicts the simulated performance [2]. Fig. 1 compares the predicted output phase noise spectrum in black and the simulated spectrum in grey; the predicted jitter is within 1% of the simulated value.

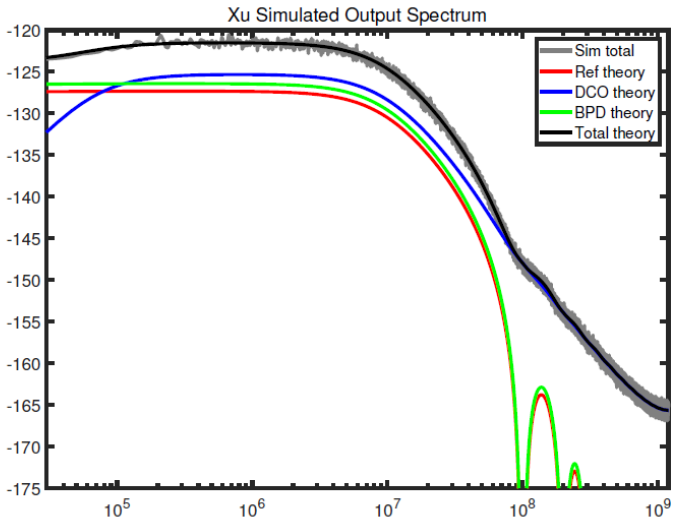

Fig. 1. Theoretical and simulated phase noise of a BB-PLL in integer-N mode [2].

Similar predictions for the fractional-N mode do not exist. We are enhancing the model by adding a multimodulus divider, DTC, and divider controller in the feedback path, as shown in Fig. 2.

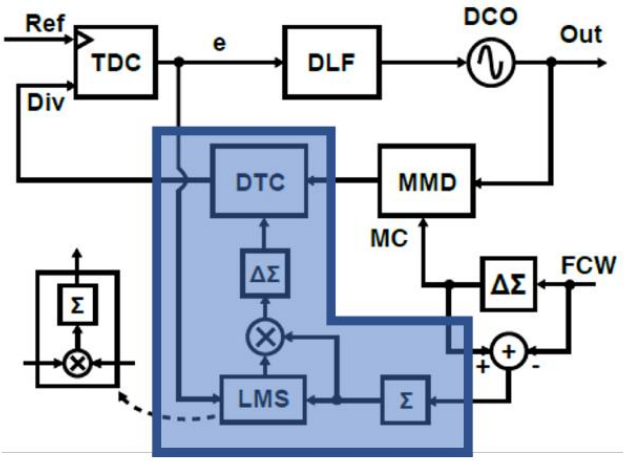

Fig. 2. Model of a fractional-N BB-PLL.

Next Steps

We will validate the phase-domain model with a conventional MASH 1-1 divider controller and then compare the fractional-N performance with that of a PMR-based divider controller.

Part II: DCO Controller (Valerio Mazzaro, Peter Kennedy)

State of the Art

To achieve high frequency resolution, a DCO is driven by a noise-shaping modulator, typically a MASH 1-1. When the shaped quantization noise of the modulator interacts with the nonlinearity of the capacitive DAC, excess spurs and folded noise are produced. The state of the art is to use *dither* to mitigate idle tones and *dynamic element matching* (DEM) to mitigate nonlinearity-induced spurs; both techniques introduce additional noise. We are using a different type of noise-shaping modulator that hopefully will both eliminate the spurs and introduce less pink noise.

Results to Date

The best model in the literature is due to Zhuang *et al.* [3]. This considers a DCO with a dithered MASH 1-1 controller and DEM. Fig. 3 shows the simulated phase noise (a) without and (b) with capacitor mismatch; the latter causes spurs and raises the pink noise floor

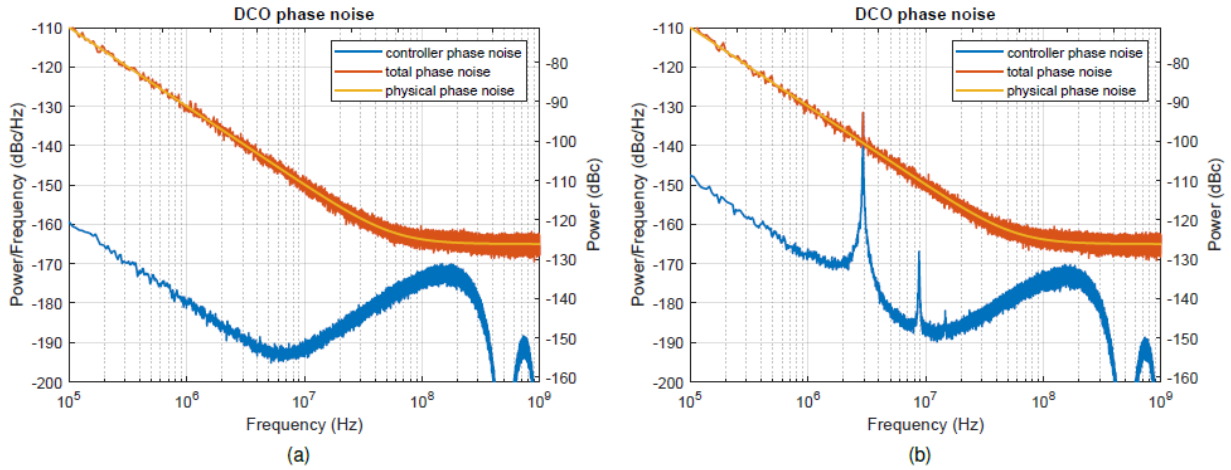

Fig. 3. DCO phase noise (a) without and (b) with capacitor mismatch.

By using DEM, the spurs in Fig. 3(b) can be mitigated, but at the cost of even more pink noise, as shown in Fig. 4. Fig. 4(a) shows the simulated phase noise in the presence of capacitor mismatch (a) with DEM and (b) with our DEM-less controller; our solution has lower folded pink noise.

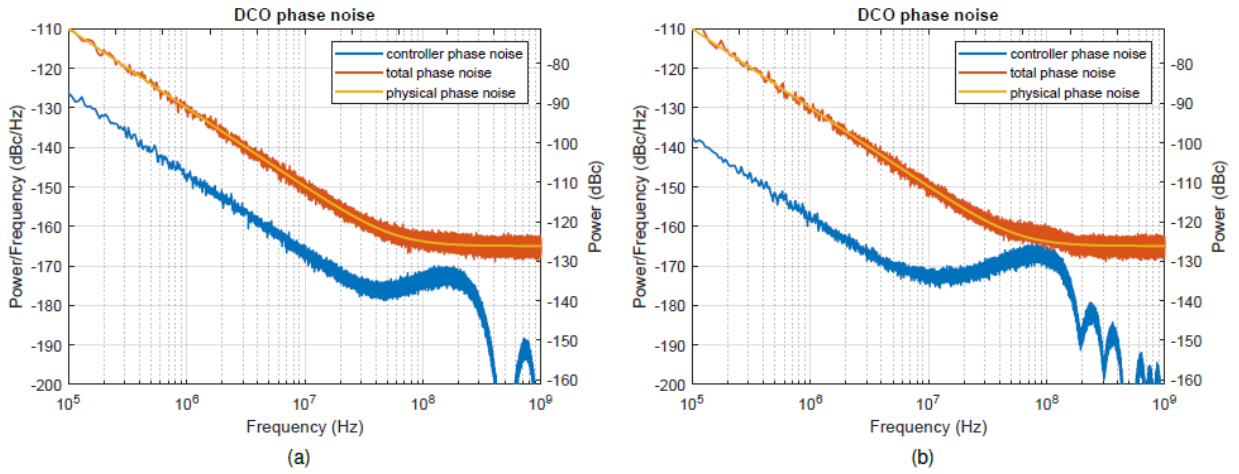

Fig. 4. Phase noise of mismatched DCO with (a) conventional and (b) novel controllers.

Lower folded pink noise offers a potential advantage in the case of low noise DCOs. Fig. 5 shows the phase noise of a DCO with a low noise corner with (a) conventional and (b) novel controllers. In Fig. 5(a), the pink noise floor is limited by the controller while it is determined by the DCO in Fig. 5(b), as one would prefer.

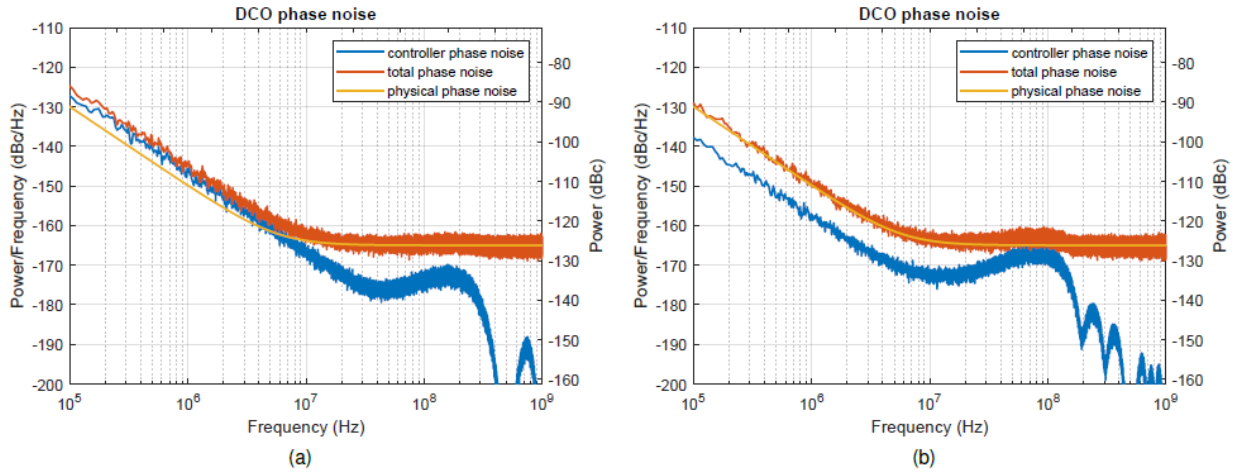

Fig. 5. Phase noise of mismatched low noise DCO with (a) conventional and (b) novel controllers.

Next Steps

We will validate the phase noise predictions of Fig. 4 by implementing the divider controllers on an FPGA and using a high-resolution DAC to emulate capacitor mismatch.

Summary

The integer-N BB-PLL model has been validated. Next, we will extend it to the fractional-N case, incorporate the PMR-based divider controller and compare the MASH and PMR solutions.

The novel DCO controller has the potential to outperform a MASH controller in the case of low-noise DCOs. Next, we will validate the performance by means of an FPGA-DAC-based emulator.

References

[1] H. Xu and A. A. Abidi, "Design Methodology for Phase-Locked Loops Using Binary (Bang-Bang) Phase Detectors," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 7, pp. 1637-1650, July 2017, doi: 10.1109/TCSI.2017.2679683.

[2] L. Avallone, M. Mercandelli, A. Santiccioli, M. P. Kennedy, S. Levantino and C. Samori, "A Comprehensive Phase Noise Analysis of Bang-Bang Digital PLLs," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 7, pp. 2775-2786, July 2021, doi: 10.1109/TCSI.2021.3072344.

[3] J. Zhuang, K. Waheed and R. B. Staszewski, "Design of Spur-Free ΣΔ Frequency Tuning Interface for Digitally Controlled Oscillators," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 1, pp. 46-50, Jan. 2015, doi: 10.1109/TCSII.2014.2362692.