A multi-sensor Analogue Frontend Using Time Domain Signal Processing

Abstract:

We live in an Internet of Things (IoT) world where our environment and vital signs are monitored by hundreds of different sensors. Each iteration of the leading Smartphones incorporate more and more sensors. A traditional multi-sensor Analogue Frontend (AFE) consists of separate channels from each sensors. Each signal path is custom designed for a particular sensor and a mux connects the individual paths to a shared ADC. This implementation takes up a lot of chip area especially if the signals need large resistors and capacitors to filter out noise above 10kHz. Analogue to Digital converters have undergone a huge increase in performance in the 21st century. These improvements have meant that the power bottleneck in sensor systems is now the analogue interface not the ADC. The circuit techniques developed in this research project will be applicable to most sensor interfaces. The project will also leverage Tyndall Sensor Technology and know-how to enable new applications in the areas such as environmental monitoring. This work is applicable to the MCCI themes of Smart Agriculture, Connected Health and Industrial.

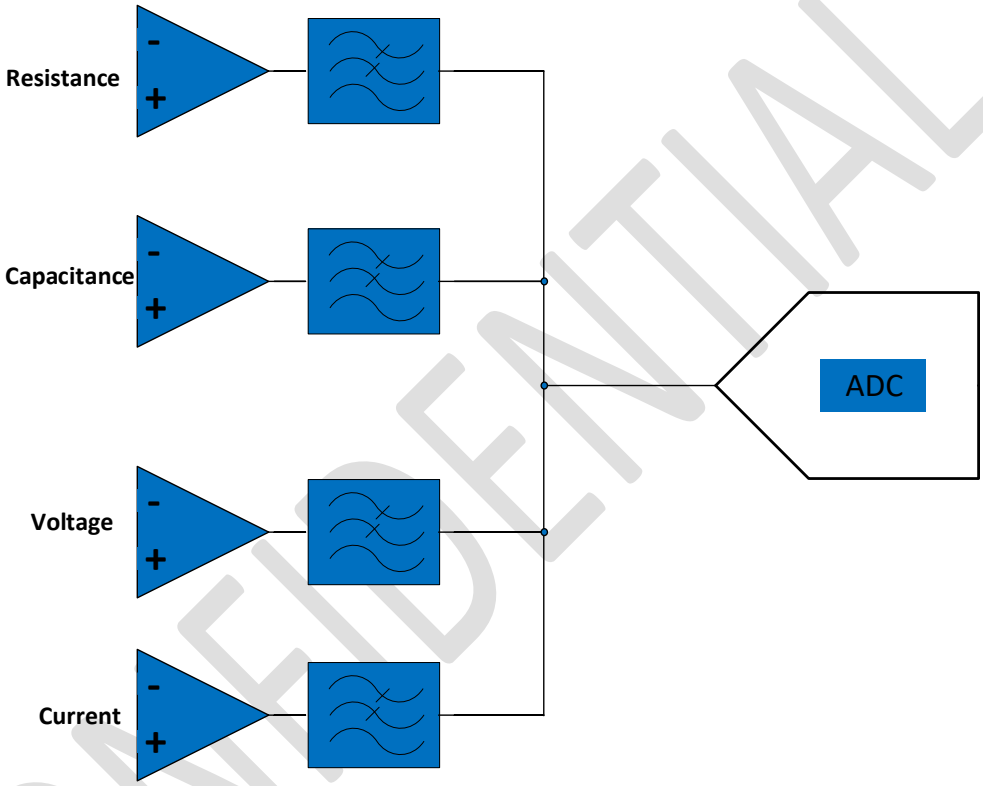
Introduction

This research project is primarily a circuits research project to design a robust adaptable sensor interface that can support Resistive, Capacitive, Voltage and Current mode sensors. A further goal will be to produce circuits that are lower in power and smaller in size than existing solutions.

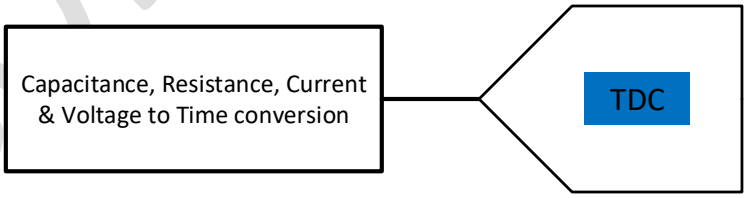
Time based signal processing uses circuit blocks such as Time to Digital Converters (TDCs), VCOs, comparators and digital logic to convert sensor signal to digital. These circuits all benefit from process scaling so the performance and power consumption will improve at advanced CMOS processes unlike conventional analogue signal processing. Fig. 1(a), shows a conventional multi-sensor AFE. The ADC is shared but each sensor path is separate. Fig. 1 (b) shows a time domain conversion circuit where the sensor signals are converted to time pulse and a TDC is used to measure the pulse. While different sensors have different voltage and frequency ranges a goal of the project will be to share circuitry

between different resistive, capacitive, voltage and current paths to produce a low area solution. Dynamic circuits and duty cycling will be employed to minimise the interface power consumption.

ADCs are only as accurate as their voltage references. Time to digital converters are only as accurate as their time references. Part of this project work will investigate low area, low power time reference circuits which can be used to calibrate the TDC circuits so absolute accuracy can be achieved by the sensor interface.



(a) Traditional Sensor AFE



(b) Combined Time domain Sensor AFE

Figure 1: Conventional Multi-Sensor Analogue Front End (AFE) (a) and a Time domain AFE (b)

Current work:

Ring based TDCs are best deployed in an oversampling architecture. This work would like to implement a closed loop topology like the Continuous Time Delta Sigma (CTDS) ADC shown in Figure 2. Feedback topologies are less susceptible to non-linearity in the circuit components. A Voltage Controlled Oscillator (VCO) or a Current Controlled Oscillator (CCO) could be used to create an oversampled phase/time signal that could be converted to digital by a TDC. VCOs and CCOs have the additional benefit that they integrate their input signal while converting to the phase output, this allows them to replace the integrators in the CTDS ADC.

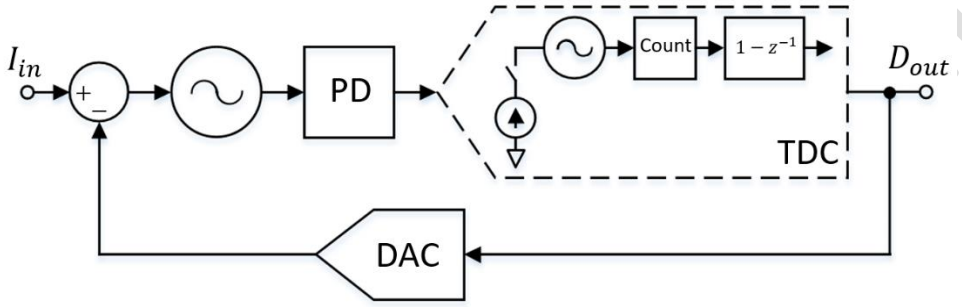


Figure 2: VCO and TDC based implementation.

The key benefits of this architecture are second order noise shaping, low power consumption and low area. Moreover, the majority of building blocks in this ADC are compatible with digital design flow. Despite the benefits mentioned above, this structure suffers from PVT variation and high-frequency spurs. PVT variation sensitivity can be compensated by using different calibration techniques. The nature of high-frequency spurs is poorly described in literature. Nevertheless, these harmonics have a huge effect on both dynamic range and stability of the system. Thus, the complete theoretical description is required. Let's have a closer look to first stage of the system depicted in Figure 2.

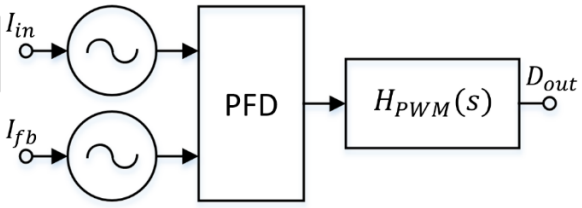


Figure 3: First stage of ADC.

The presence of phase-to-frequency detector as phase comparator results in pulse-width modulated signal at the input of quantizer. The high-order PWM components folds into the band because of aliasing. Figure 5 shows the spectrum of PWM signal (a), output signal spectrum with (c) and without (b) aliasing.

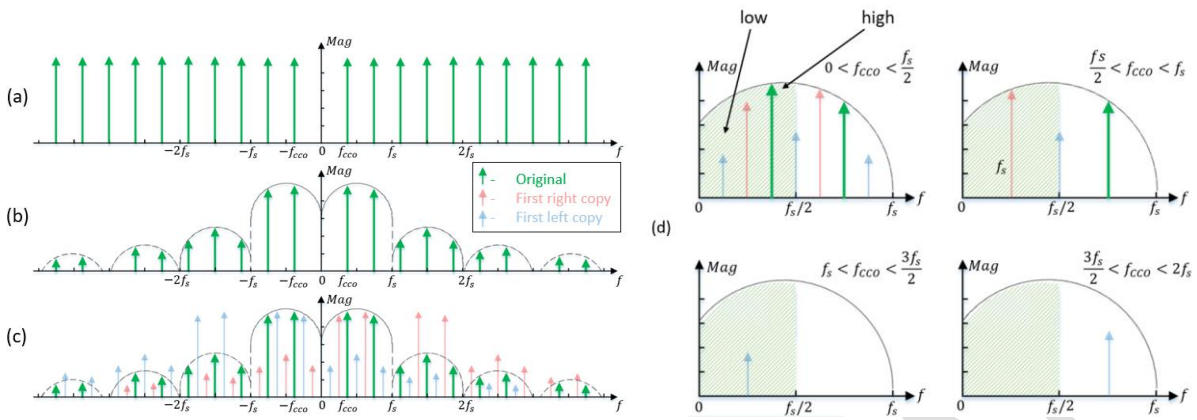


Figure 4: PWM tones in-band folding

The distribution of PWM tones depends on free running frequency of the first VCO stage. Four different tone distributions for different VCO free-running frequencies are shown in Figure 4(d). Meanwhile, this parameter is affecting the phase margin of the system. The simulation results are shown in Figure 5

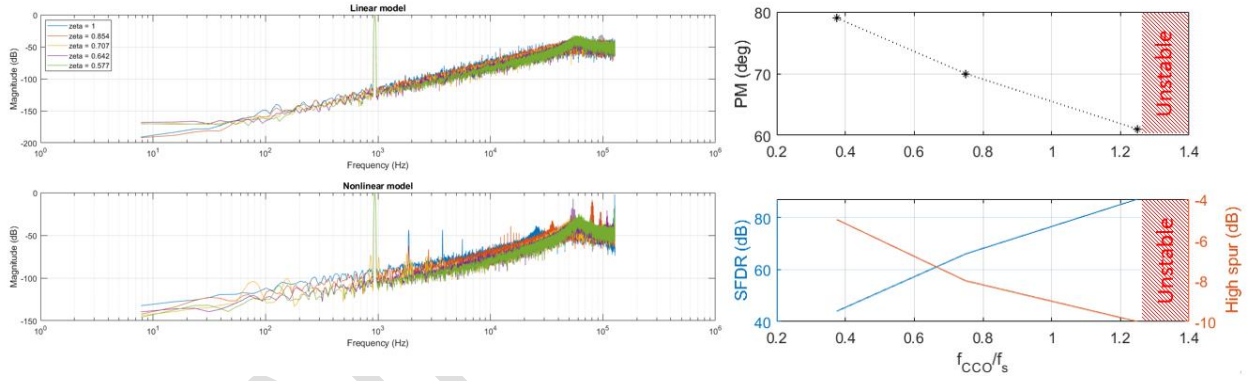


Figure 5: VCO and TDC based implementation simulation results.

Figure 5 represents the trade-off between phase margin and dynamic range of the ADC. Phase averaging is one of the proposed techniques to solve that issue [3]. The models built for this project allow different VCO frequencies and phase averaging to be investigated to find suitable regions of operation. The models have been updated with thermal noise, jitter and block non-linearity's added. Figure 6 shows a block diagram with different noise sources added and Figure 7 shows non-linear models added for the VCO and the feedback DAC.

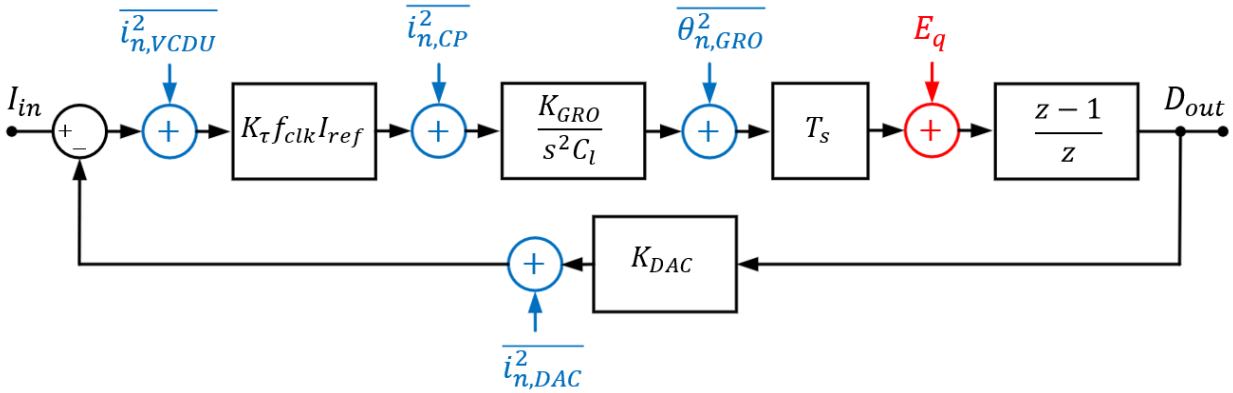


Figure 6: Noise sources model

The models have allowed the block constraints to be investigated and specifications to be determined for the building blocks. Schematic design is underway to design the sub-blocks and implement an improved ADC topology.

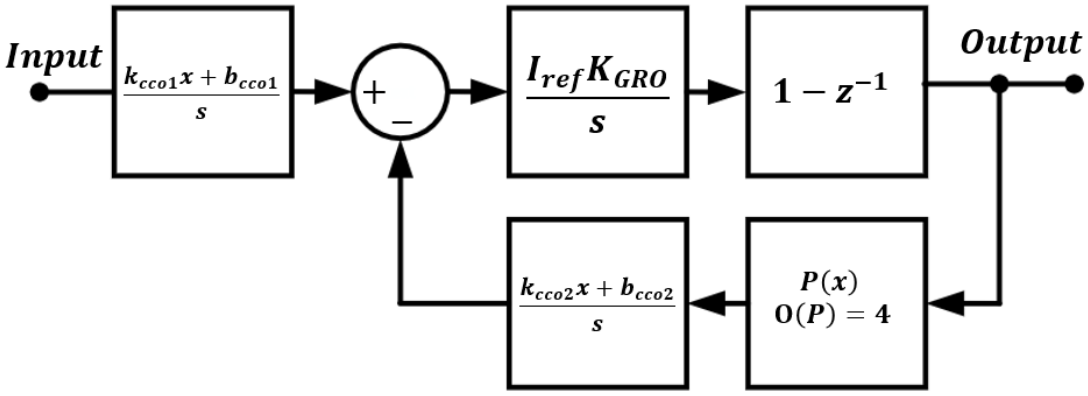


Figure 7: Non-linearity's model

References

[1] M. Z. Straayer and M. H. Perrott, "A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping," in *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1089-1098, April 2009, doi: 10.1109/JSSC.2009.2014709.

[2] A. Elshazly, S. Rao, B. Young and P. K. Hanumolu, "A Noise-Shaping Time-to-Digital Converter Using Switched-Ring Oscillators—Analysis, Design, and Measurement Techniques," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 5, pp. 1184-1197, May 2014, doi: 10.1109/JSSC.2014.2305651.

[3] C. Pochet, J. Huang, P. P. Mercier and D. A. Hall, "28.4 A 400mVpp 92.3 dB-SNDR 1kHz-BW 2nd-Order VCO-Based ExG-to-Digital Front-End Using a Multiphase Gated-Inverted Ring-Oscillator Quantizer," *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, 2021, pp. 392-394, doi: 10.1109/ISSCC42613.2021.9365985.

[4] C. Pochet and D. A. Hall, "A 4.4μW 2.5kHz-BW 92.1dB-SNDR 3rd-Order VCO-Based ADC With Pseudo Virtual Ground Feedforward Linearization," *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, 2022, pp. 408-410, doi: 10.1109/ISSCC42614.2022.9731549.