Novel Modulators for Low-Spur BB-PLLs

Abstract

This project is in two parts: (i) development of a modulator controller that, when incorporated in a fractional-N BB-PLL, produces lower spurs and noise than a MASH-based controller and (ii) development of a DCO controller that produces lower noise and spurs than a conventional MASH-based controller. This report summarizes progress over the past twelve months.

Introduction

BB-PLLs are cheap and easy to implement but suffer from a range of problems associated with nonlinear components. Apart from noise due to physical components, there are at least four sources of quantization noise: the bang-bang phase detector, the DCO and, in the case of a fractional-N frequency synthesis, the modulator and DTC that implement fractional division.

Quantization noise is fundamentally mathematical in nature. We will use mathematics to mitigate/eliminate it. The core technique we will exploit is PMR, which we demonstrated in a CP-PLL and set a new record at ISSCC 2019 for measured worst-case inband fractional spurs. KAIST presented a variant of PMR at ISSCC 2020 that set a new record for worst-case inband fractional spurs in an ADPLL with a ring DCO.

Fractional-N BB-PLLs still lag significantly behind CP-PLLs in terms of their spur performance. This work will help us to close the gap.

The project is in two parts: (i) development of a modulator controller that, when incorporated in a fractional-N BB-PLL, produces lower spurs and noise than a MASH-based controller and (ii) development of a DCO controller that produces lower noise and spurs than a conventional MASH-based controller.

Luca Avallone and Xu Wang have been addressing the modulator that enables fractional-N division and interacts with the bang-bang nonlinearity. High-level models of the BB-PLL have been designed and validated at system level. Luca Avallone graduated after publishing the integer-N model; he joined Infineon. Xu Wang took a break from his studies in Spring 2022; he has been working on the fractional-N extension since July 2022.

Valerio Mazzaro worked on the DCO and its modulator. He has developed, simulated and filed a patent application for a novel spur-free divider controller architecture for the DCO. We presented this work at the MCCI MTC. Valerio Mazzaro took up full-time employment with STMicroelectronics in May 2022. An ME student was working on an FPGA implementation but dropped out; a BE student, Danylo Galach, is now working on this part.

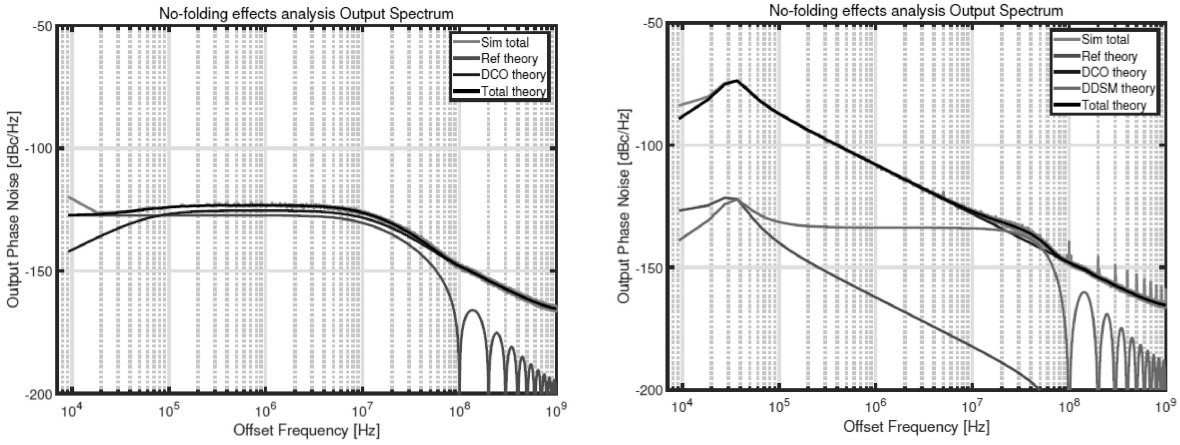
Part I: Feedback Divider Controller (Luca Avallone, Xu Wang, Peter Kennedy)

State of the Art

Until 2021, the best model of an integer-N bang-bang PLL in the literature was that due to Xu and Abidi [1]. Luca Avallone published a superior high-level theoretical model that accurately predicts the simulated performance [2]. Similar predictions for the fractional-N mode have not been available in the literature.

Results to Date

Since July 2022, Xu Wang has validated the integer-N ADPLL model that was built by Luca Avallone (Fig. 1(a)). He has added a multimodulus divider and a divider controller in the feedback path and has matched his new theoretical model to simulations in the case of a fractional-N ADPLL without a DTC (Fig. 1(b)). The extended model can handle a variety of phase detectors including multi-level TDCs and a BBPD.



(a) (b)

Fig. 1. Output phase noise of (a) integer-N and (b) fractional-N ADPLLs showing match between analytical predictions (black) and simulations (grey).

Next Steps

Xu Wang will next add a DTC to bring the performance of the fractional-N ADPLL closer to that of the integer-N variant and then introduce a PMR-based divider controller to mitigate the residual nonlinearities.

We plan to publish the new model in *IEEE Transactions on Circuits and Systems* and ultimately to seek a partner with whom to implement the proposed PMR-based ADPLL.

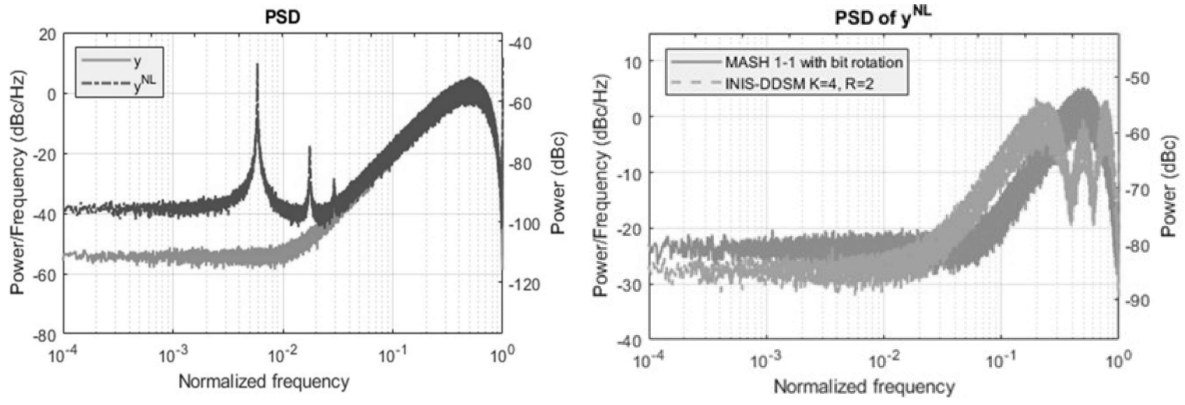
Part II: DCO Controller (Valerio Mazzaro, Danylo Galach, Peter Kennedy)

State of the Art

To achieve high frequency resolution, a DCO is driven by a noise-shaping modulator, typically a MASH 1-1. When the shaped quantization noise of the modulator interacts with the nonlinearity of the capacitive DAC, excess spurs and folded noise are produced. The state of the art is to use *dither* to mitigate idle tones and *dynamic element matching* (DEM) to mitigate nonlinearity-induced spurs [3]; both techniques introduce additional noise. We are using a different type of noise-shaping modulator that hopefully will both eliminate the spurs and introduce less pink noise [4].

Results to Date

The distorted output of a MASH 1-1 contains an elevated noise floor and spurs, as shown in purple in Fig. 2(a). With a DEM scheme such as bit rotation, the spurs can be mitigated, but the noise floor is further elevated, as shown in orange in Fig. 2(b). Simulations confirm the theoretical prediction that our modified DDSM (denoted INIS-DDSM [5]) is also spur-free; in addition, it has a significantly lower noise floor than the MASH 1-1 with a bit rotator.



(a) (b)

Fig. 2. (a) Output of a dithered MASH 1-1 before and after nonlinear distortion and (b) outputs of the distorted outputs of a MASH 1-1 with bit rotation and an INIS-DDSM, both of which are spur-free.

Next Steps

BE student Danylo Galach will validate the spectral predictions of Fig. 2 by implementing the MASH 1-1 and INIS-DDSM on an FPGA (Spartan 6) and using a high-resolution DAC (AD9767) to emulate capacitor mismatch in a DCO.

Summary

The integer-N and basic fractional-N BB-PLL models have been validated. Next, we will add the DTC to the fractional-N model, incorporate the PMR-based divider controller and compare the MASH and PMR solutions.

The INIS-DDSM has the potential to outperform a MASH controller in the case of low-noise DCOs. We will validate the performance by means of an FPGA-DAC-based emulator.

References

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[5] V. Mazzaro and M.P. Kennedy. A Family of ΔΣ Modulators with High Spur Immunity and Low Folded Noise When Used in Fractional-N Frequency Synthesizers. *IEEE Trans. Circuits and Systems-Part I*, 69(11):4499-4509, Nov. 2022. doi: 10.1109/TCSI.2022.3195659

[4] V. Mazzaro and M.P. Kennedy. “Digital delta sigma modulator with inherent spur immunity after nonlinear distortion,” U.S. Patent application, 11 April 2022.