CMOS Voltage and Time References for Cryogenic Applications

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Abstract: The polar Bear project aims to design time and voltage CMOS references capable of working in the 4°K temperature regime for quantum computing applications. This first report presents the integrated circuit designs chosen to characterise the TSMC 65nm CMOS process. Those circuits include standalone NMOS, PMOS and resistors, along with bandgap references and ring oscillators. The testing plan and instrumentation is also briefly discussed.
Keywords: **Cryo-CMOS, Quantum Computing, 4°K, Bandgap-Reference, Ring-Oscillator, CMOS**.

1. Introduction

The core of quantum computers are the quantum processors that operate with quantum bits (qubits). Quantum processors operate at near absolute zero temperature, between 20 and 230°mK, in order to take advantage of the quantum properties of the materials employed for their implementation. On the other hand, the quantum processor's readout interfaces operate at room temperature, 273°K. This imposes integration limitations due to the gap in operating temperatures and the large amount of wires used to interface each qubit with the readout circuits. Recently, Cryogenic CMOS (Cryo-CMOS) circuits operating at cryogenic temperatures, typically around 4K, are emerging in the implementation and integration of the readout circuits for quantum processors [1]. A typical quantum processor interface implemented with Cryo-CMOS circuits is illustrated in Fig. 1

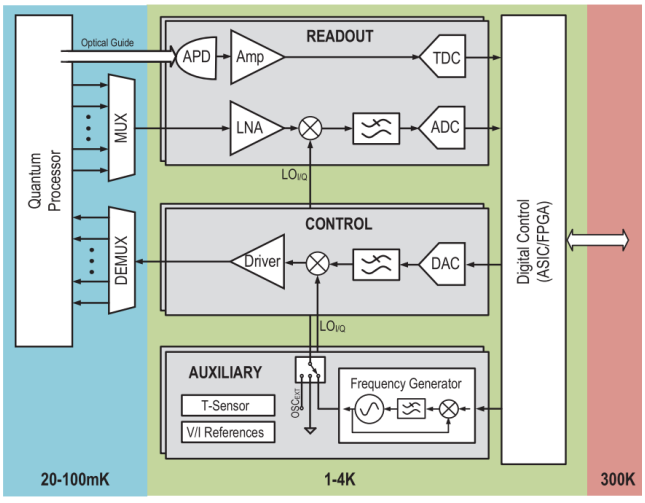

Fig. 1 Quantum processor interface using Cryo-CMOS circuits as presented in [1].

[1]. This interface resembles a radio transmitter, where the control circuitry works based on sending a high frequency pulse to stimulate the qubit, while the readout circuit acts as a receiver that listen to the qubit response. Several key building blocks can be identified, such as: Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs), Time-to-Digital Converters (TDCs), analog mixers, voltage and time/frequency references. The later, voltage and time/frequency references are essential to ensure adequate operation of the rest of circuitry in the interface, and therefore are of great importance. The polar Bear project aims to design time and voltage CMOS references capable of working in the 4°K temperature regime.

2. CMOS Circuits to characterise the 65nm technology

Although CMOS technologies are very mature and reliable when used in the temperature range of 233°K – 373°K, foundries do not provide valid transistor models for cryogenic temperatures. Therefore, Cryo-CMOS Integrated Circuit (IC) design always starts with the transistor and basic building blocks characterisation at 4°K [2]-[3]. This research work will initially focus on the characterisation of standalone transistors, simple bandgap references and frequency references.

In order to characterise the 65nm CMOS process at 4°K, the first Integrated Circuit (IC) design comprises standalone PMOS and NMOS transistors of different widths and types, general purpose, thick oxide, etc. The aim is to obtain I/V curves at room temperature and at 4°K, in order to extrapolate the threshold voltage of MOS devices at cryogenic temperatures. Similarly, resistors of different types are integrated in order to characterize them at cryogenic temperatures.

Bandgap references with the topology shown in Fig. 2, [4], are also integrated. Several variations are used in order to obtain as much data as possible from the IC functioning under the 4°K temperature regime. The set of BGRs includes: PNP as core (IO CMOS for the rest), IO PMOS as core (IO CMOS for the rest), Standard CMOS as core (standard CMOS for the rest), LVT CMOS as core (LVT COMSs for the rest), and LVT DTCMOS as core (LVT DTCMOSs for the rest). Finally, two ring oscillators are also included in the IC in order to use them as time/frequency references and verify functionality of digital circuits at low temperatures. The ring oscillator is made-up 20 digital CMOS inverters. A clock divider, by 256, is also used to slowdown the output rate. The chip was successfully taped out in Q2 2022, and the packaged parts are expected for Q4 2024.

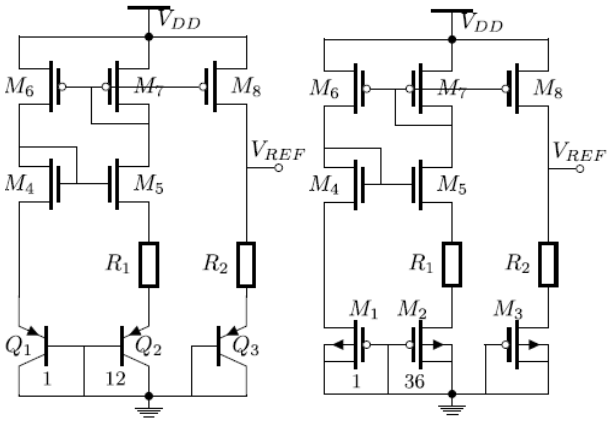

Fig. 2 BGR Circuits (left-PNP, right-MOSFET) [4].

3. Testing Plan

A Bluefors 4K system will be used to cool the IC design down to 4°K. Two R&S HMP4040 power supplies and one Keysight 34465A multimeter will be used to obtain transistor's I/V curves and measure the bandgap references. A Python script is under development to automate the test measurements of the IV curves. The plan is to take measurements at 10°K intervals from 300K down to 4K in order to characterise the different devices and circuits.

References

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