Ultra-low Power Sensor interface for Biomedical Application

Abstract:

The proposed SAR ADC introduces a switched supply based comparator, which reduces the effective supply voltage of the comparator during the decision phase, without the requirement of a dedicated DC-DC down converter, pin or external supply rail. The proposed comparator achieves a 28 % power consumption reduction when compared to the conventional designs. In addition, the design utilizes a clock boosting circuit instead of a boot-strapped switch on the input switch, without degrading the achievable SNDR and also achieves 46% power consumption reduction compared to bootstrap switch. Synchronous low power handcrafted logic is used to further reduce the power consumption. The 14b SAR ADC was fabricated in 65nm CMOS and consumes 9.14 µW from a 1V supply and achieves an SNDR of 71.7 dB at 0.5 MS/s resulting in a Walden FOM of 5.7 fJ/Conv

Proposed ADC architecture:

In energy constrained edge devices, ultra-low power operation is a critical consideration when operating from a lifetime battery or an energy harvesting source. In such applications it is important to ensure that all the sub-blocks are optimally powered, which means that the sub-blocks are provided with just enough energy to complete their task and no more.

This work aims to reduce the power in a SAR, by reducing the supply voltage from 1.2V in standard 65nm to 0.5V, without reduction in performance. Our approach is to first design each of the blocks with "just" enough power, run the various blocks at the appropriate voltage and eliminate any wasted power. Once each of the blocks are designed for just the power required to make decision, the next step is to employ voltage boosting technique to boost each of the blocks to the optimum voltage required for operation. Low powered TSPC LOGIC is designed

which can operate at 500mV supply, then boost this supply voltage given to logic to required voltage for each of the blocks. Switched Supply technique is applied to the comparator, while having minimal reduction in performance even when confronted with significant power supply noise.

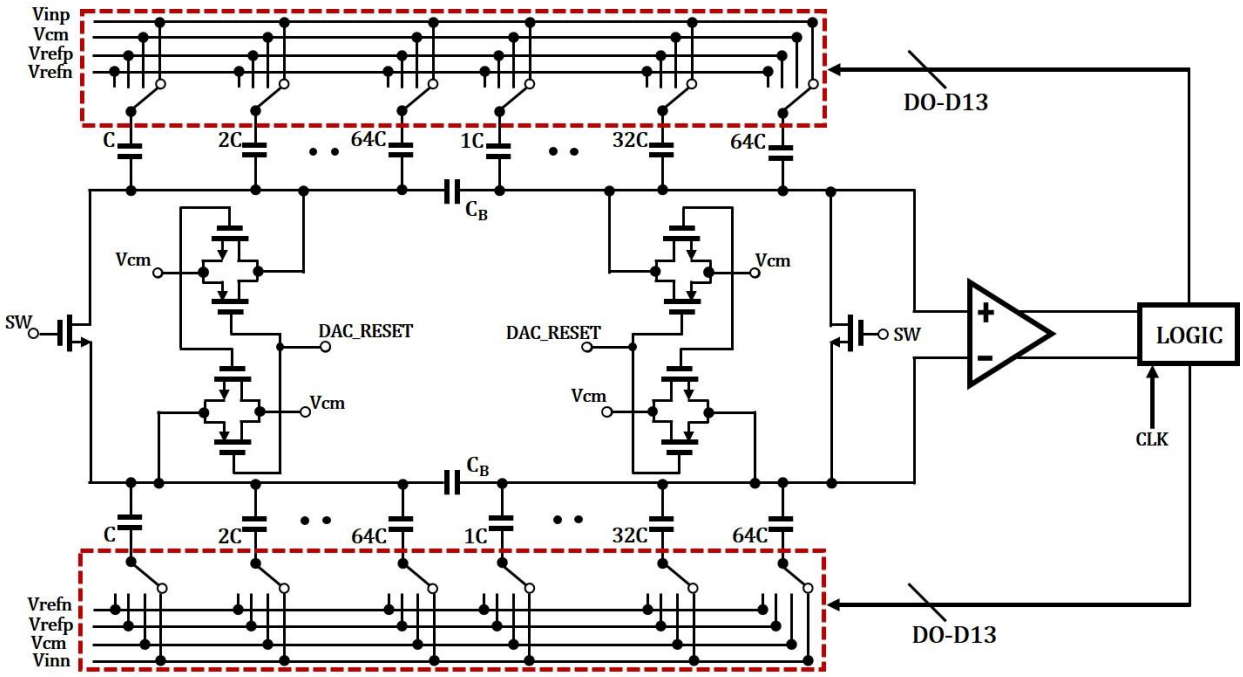


Fig .1. Proposed 14 bit SAR ADC, with Switched Supply comparator, NMOS Clock Boosted driven input sampling switches and hand crafted TSPC logic

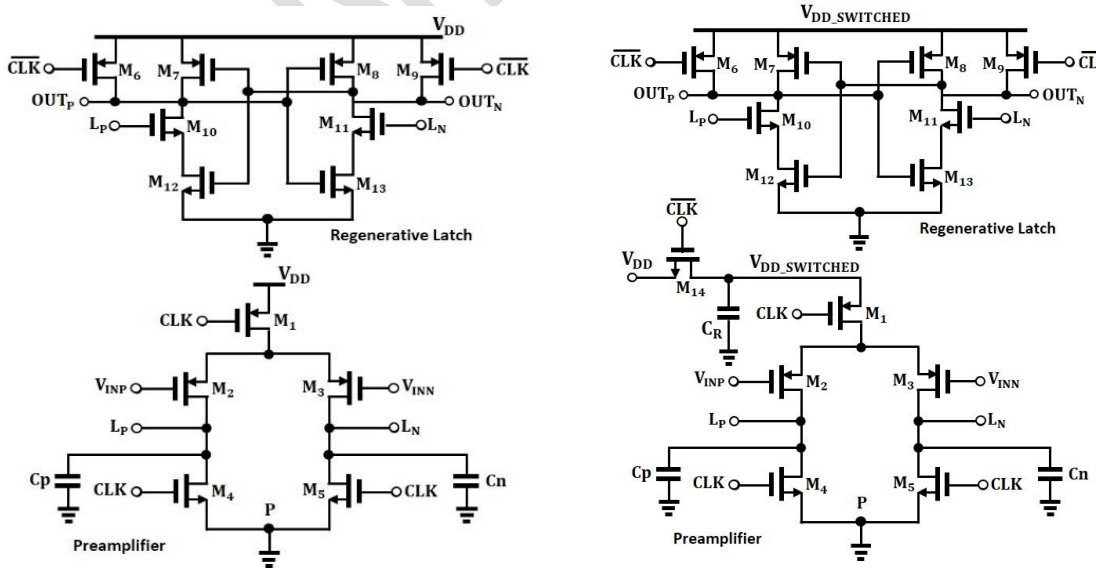


Fig.2. Conventional and Proposed comparator architecture.

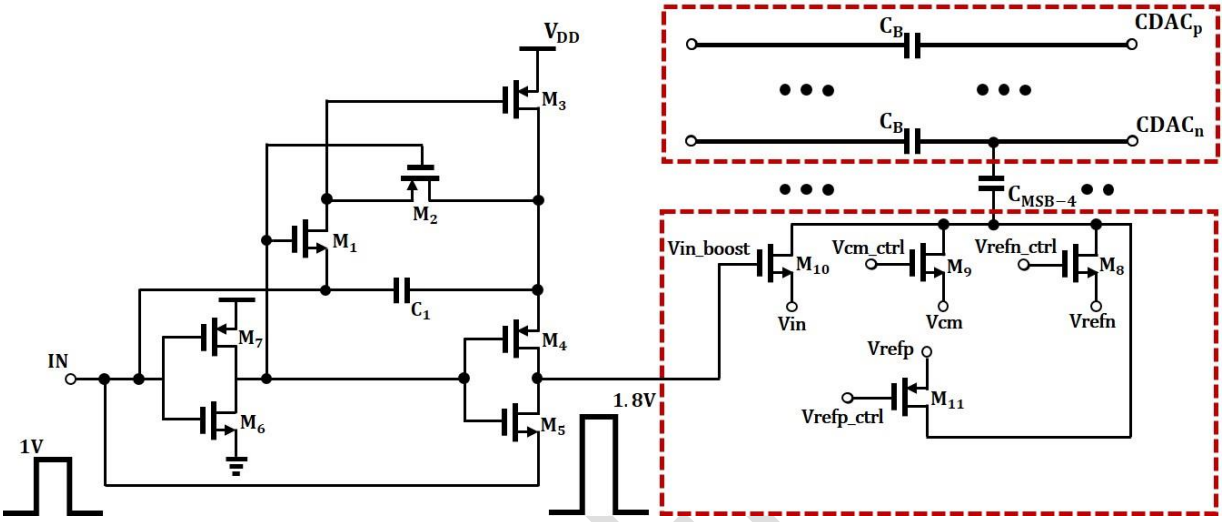


Fig.3. Clock boosting circit used to sample the input instead of bootstrap switch

Shrew testing update:

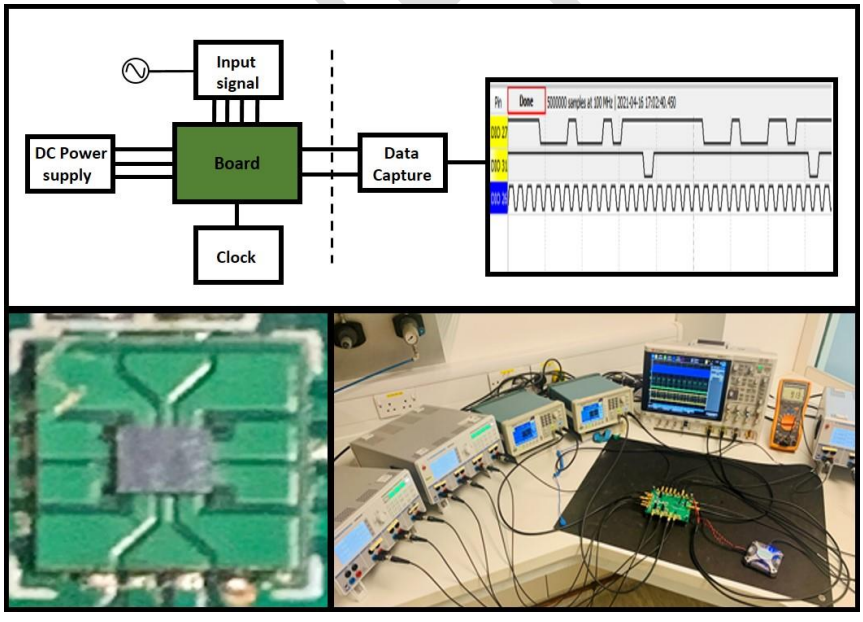
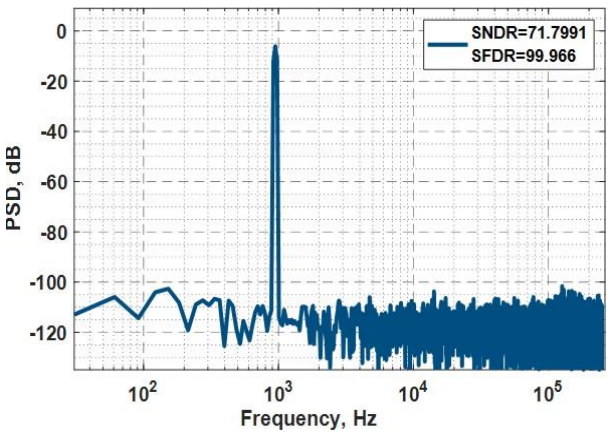


Fig.4 . Measurement and Evaluation setup of SAR ADC.



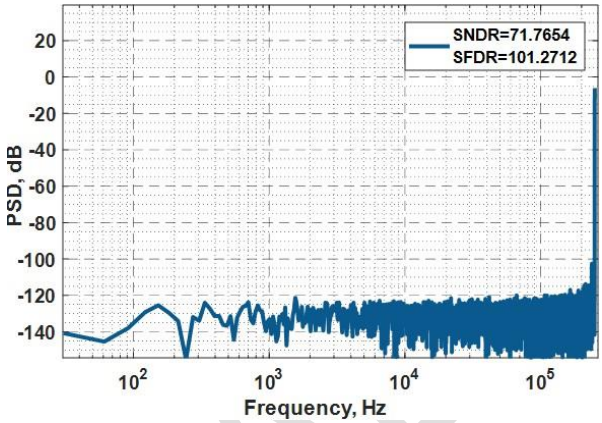


Fig.5. FFT of the measured ADC output, Fin = 946.00449219 Hz, 16384 bins, FFT of the measured ADC output, Fin = 249.9694824 KHz, 16384 bins.

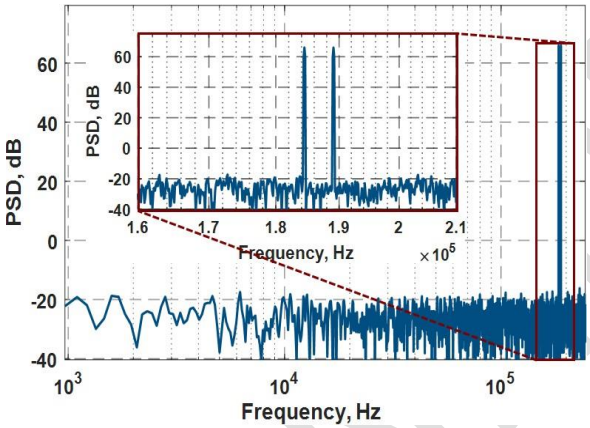


Fig.7. Two tone measurement test.

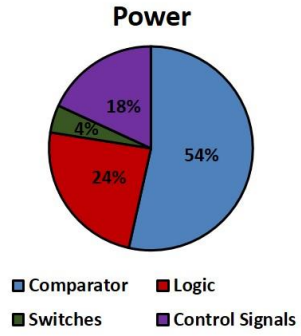


Fig.8. power breakdown of SAR ADC

parameter	This work
Technology	65nm
Supply	1V
Sample rate [S/s]	0.5M
Power [W]	9.14μ
SNDR [dB]	71.8
SFDR [dB]	101.2
FoMs [dB]	176.2

FOMw [FJ/Conv]	**5.7**
Input sampling	**Clock boosting**

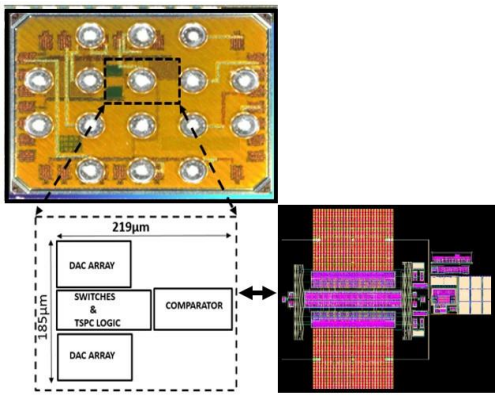


Fig.8. Die micrograph

Performance summary

Programmable switch supply comparator

- Programmable switch supply comparator, which reduces the effective supply voltage of the comparator during the decision phase, without the requirement of dedicated DC-DC converter, pin or external or supply rail. The proposed comparator achieves up to 50 % power consumption reduction compared to conventional designs and can replace the coarse and fine comparator in SAR ADC shown in Fig .9. Without the need of offset calibration. In addition the proposed design gives extra degree of freedom to control noise, power and speed of both PMOS and NMOS input switch supply programmable comparator. The proposed PMOS and NMOS switch supply comparator was fabricated in 65 nm CMOS process. The PMOS input pair consumes 2.24 to 3.75uW from 1V supply and achieves an input referred noise voltage of 90uV to 205uV.

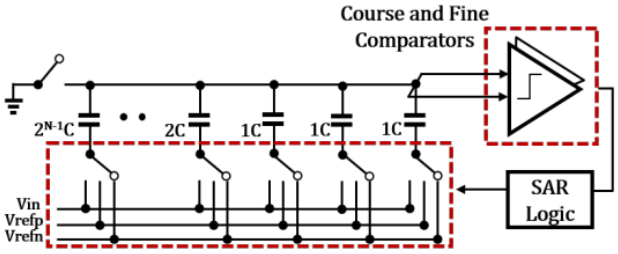


Fig.9. Two comparator architecture

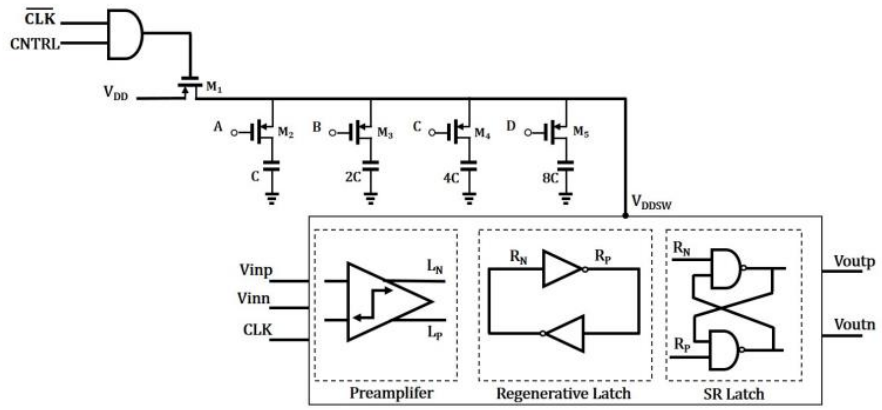


Fig.9. proposed architecture

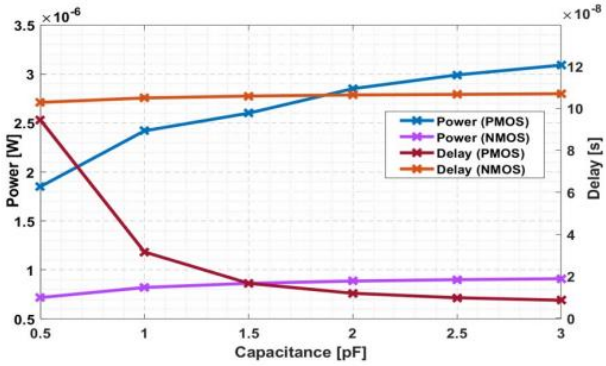


Fig.9. power delay plot of both pmos and nmos input CR

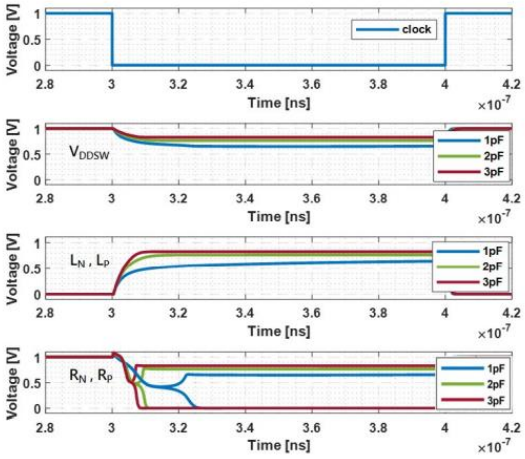
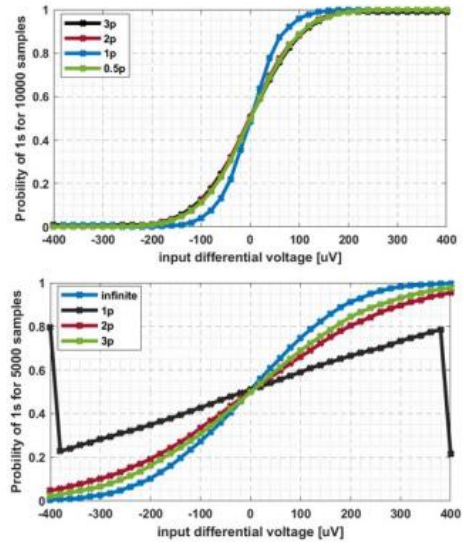


Fig.9. Timing diagram of pmos input with variable



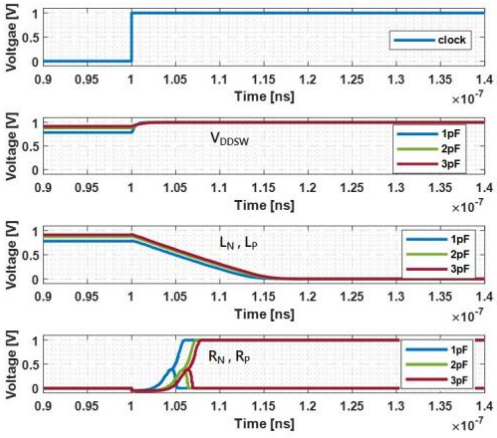


Fig.9. RMS noise of both pmos and nmos input type CR

Fig.9. Timing diagram of nmos input with variable

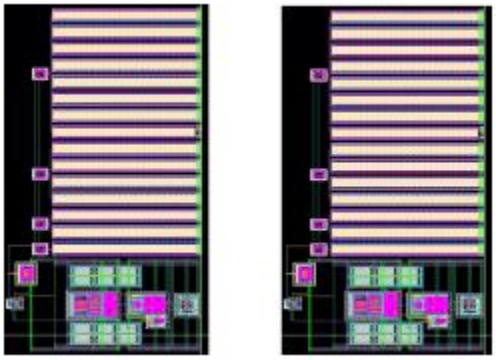


Fig.9.Layout of the Two proposed comparator architecture.

Future work.

- Submit the 1V SAR ADC paper to SSCL.
- Test the programmable comparator and submit the results to SSCL.
- Submit the ping pong based SAR ADC to electronic letters.