
ANNUAL
REPORT
2024
MCCI
MICROELECTRONIC CIRCUITS CENTRE IRELAND
TECHNOLOGY
CENTRE
ENTERPRISE IRELAND
IDA IRELAND SUPPORTED

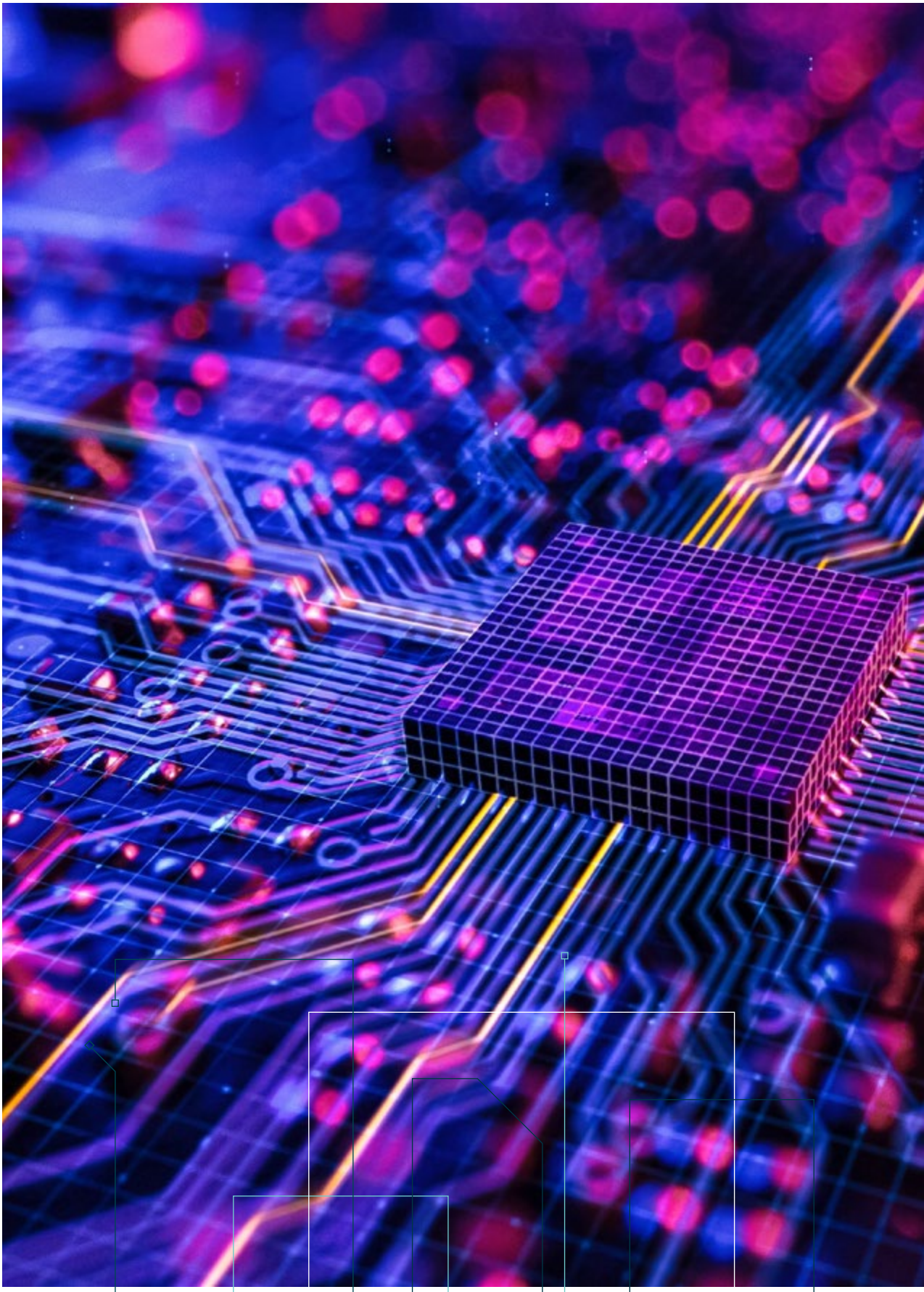


Table of contents

Executive Director's Message	4
Chairperson's Message	6
About Us	9
Our Mission and Impact	10
Research Pillars	12
Application Areas	16
Researcher Profiles	20
Research Publications	28

Executive Director's Message

I am delighted to present the 2024 Annual Report for Microelectronic Circuits Centre Ireland (MCCI). This year has been defined by significant strategic progress, successful research outputs and growing recognition of Ireland's role in the global semiconductor ecosystem. Our continued commitment to excellence in microelectronic IC design research, innovation and collaboration has reinforced MCCI's position as a critical enabler of advanced technology development in Ireland.

One key highlight was Prof. Michael Peter Kennedy and Valerio Mazzaro's paper being accepted at IEEE ISSCC 2024, which is fantastic for Prof Kennedy, UCD researchers and the MCCI team. The ground-breaking paper and its work was developed in close collaboration with ADI Limerick RF team, entitled "A 45.5fs Integrated Random Jitter and 75dBc Integer Boundary Spur BiCMOS Fractional PLL with Suppression of Fractional, Horn and Wandering Spur," was presented at the conference by Prof Kennedy in February 2024 and was very well received. The year was also marked by expert research talent recruitment, where I was delighted to appoint, Dr. Vishal Jagtap as Head of Group of MCCI's team at Tyndall National Institute and Dr. Hugo Cruz joined as new Principal Investigator in the Integrated Power Systems group.

The group has achieved many significant milestones during the year. Specifically in competitive funding, with a significant grant award from EU EDF project "e-PERFECT" by Dr. Vishal Jagtap. A 40 month project duration, with a theme of EDF-2024-RA-SI-MATCOMP-EC and comprises of 13 partners across Europe with some well know primes involved. This is a very significant award as it bring MCCI into focus in a large EU EDF consortium which offers many new possibilities for new EU funding going forward. This was followed by an Enterprise Ireland grant award for MCCI's submission to the EI "Work Ready Program". The object is to help with the work internship placement and training of college graduates into the workplace for a 1 year duration, especially to help the SME community in the sector.

The MCCI group has been running 49 research projects in total during Phase 3 period (2020-2025), with 19 completed successfully by the end of this year 2024, with the remaining 30 active project due for completion by end of 2025. From the projects completed to date, 23 IEEE tier 1 publications have been achieved during 2024 bringing the MCCI cumulative total to 206 and has resulted in 118 trained researchers transferred to Industry with 70% staying in jobs in companies based in Ireland. These are important metrics for MCCI and Enterprise Ireland and the semiconductor sector in general. During 2024 we have engaged and worked directly with more SMEs, which is important for MCCI and the sector. Truly an excellent year of achievements in MCCI 14 year history, with a lot more to deliver on across the board for 2025 and the future.

MCCI was invited, among other research and academic institutes, industry sector members and state agencies by the Department of Enterprise Trade and Employment (DETE) to contribute to the public consultation on the development of Ireland's National Semiconductor Strategy. This important initiative, launched in early 2024, will help define Ireland's national priorities and aspirations in the semiconductor space and align them

with the EU CHIP JU strategy and opportunities for leadership. We welcomed the opportunity to engage with stakeholders across academia, industry, and government, contributing insights across key themes such as access to talent, barriers to growth, and sectoral opportunities and look forward to the launch of the National Semiconductor Strategy in due course in 2025.

In October 2024, Tyndall, in partnership with MCCI, MIDAS Ireland and UCD/NovaUCD, and with the approval of the Department of Enterprise Trade and Employment (DETE) submitted a landmark submission proposal to the CHIPS Joint Undertaking (JU) for an Irish Semiconductor Competence Centre called "I-C3". These EU Competences Centres when approved and set up, are to exist as national hubs, established under the European Chips JU, that provide local businesses, especially SMEs and start-ups, with expertise, training, funding, and access to cutting-edge European semiconductor design and pilot line facilities to accelerate innovation. These centres, with the first wave launching in 2025 will act as a crucial entry point into the broader EU semiconductor ecosystem, fostering skills development and supporting companies in developing and testing new semiconductor solutions. Each center specializes in different areas, creating a Union-wide network for knowledge sharing and strengthening Europe's semiconductor capabilities. The Irish submission for "I-C3 " was successful and will receive grants from both EU and the Irish Exchequer to begin set-up and become operational in mid-2025. I-C3 will be hosted in Tyndall and MCCI is an active consortium partner in its establishment and operation going forward. This pan-national effort signals Ireland's readiness to play a leadership role in the future EU semiconductor landscape.

During 2024, MCCI has begun planning for the next 5 year (2025-2030) roadmap of research and development activity and further growth phase of MCCI that will become an integral part of the new Phase 4 business plan development for submission to the Enterprise Ireland Technology Centre Program during 2025. Discussions have begun with EI Tech Centre management on this in preparation for the final Phase 4 submission during 2025. The pre-work on the Phase 4 Research and Development Strategy is in partnership with Industry members and MCCI's external expert technical review panel (Technical Steering Group) reviews and scoring in terms of alignment and strategic importance to the sector. The Phase 4 proposal drafts have and will continue to been reviewed and approved by MCCI's Central Steering Committee and by EI. Final Drafts of Phase 4 Business Plan submission will be approved by all stake holders and concluded in 2025 before formal submission to EI in 2025. Enterprise Ireland is developing its own new 5 year strategy and the EI Technology Centre Program is also evolving with-in this overall EI strategy which is expected to be launched in early 2025. It is expected that MCCI will await this launch by EI before making its final Phase4 Business plan submission.

John Morrissey
Executive Director,
Microelectronic Circuits Centre
Ireland (MCCI)

Chairperson's Message

In 2024, MCCI continues to build on its role as a key contributor to research and development in semiconductor technologies. Operating as a €10 million per annum research centre, MCCI brings together a team of nearly 90 researchers working on microelectronics innovation here in Ireland.

At the core of MCCI's success is its people, dedicated teams led by experienced researchers who focus on developing system level solutions to address practical challenges faced by industry. Supporting the development of skilled talent continues to be a priority, as we work to help maintain and grow Ireland's presence in the global semiconductor landscape. As part of the Tyndall National Institute, MCCI collaborates closely with research groups across disciplines including Photonics, Materials Science, Electrochemistry and Medical Devices. This multidisciplinary environment supports integrated research and provides a strong foundation for continued development. MCCI is committed to contributing to these efforts, supporting Ireland's goals within a broader European context. Through continued collaboration and a focus on impactful research, we aim to help strengthen the foundation of a sustainable and competitive semiconductor sector.

Donal Sullivan
Chairman,
Microelectronic Circuits Centre Ireland (MCCI)

About Us

At MCCI, our vision is to be a globally recognised leader in microelectronic integrated circuit (IC) design research and to grow as a centre of international excellence.

What sets us apart is our deep commitment to industry-academic collaboration. This approach ensures our research is not only globally competitive but also directly impactful and aligned with real-world needs. We've built strong partnerships with leading semiconductor companies such as ADI, AMD, Qualcomm, Infineon, Qorvo and Cadence.

Expanding on this foundation, we're extending our reach into application focused technology development across a variety of sectors including biotech, medtech, energy and power management and smart agriculture. Through collaboration with Irish SME's like Altratech, BCON Medical, Luma Vision, Equal1, Mindseed, and Medtech company Boston Scientifc, we're diversifying our research focus and increasing our impact across new and emerging domains.

Our mission is to enable cutting-edge technology innovation through collaborative industry partnerships that deliver meaningful societal and environmental benefits. In parallel, we're committed to developing the next generation of leaders in the global semiconductor industry.

Our strategic goals centre on excellence in microelectronics research, industry relevance, talent development and effective technology transfer. As the technology landscape continues to evolve rapidly, we are focused on:

- Broadening our research strategy in core and emerging areas.
- Deepening industry alignment to remain responsive to market needs.
- Elevating research quality through Tier 1 publications.
- Scaling our efforts for greater impact and reach.
- Increasing the number of industry transitions and improving access to research IP.

With this forward-looking approach, MCCI is driving innovation, shaping the future of microelectronics and contributing to Ireland's and Europe's leadership in semiconductor technologies.

Our Mission and Impact

MCCI's mission is to deliver high-impact research outcomes while developing independent thinkers and future leaders for both Irish enterprises and the global semiconductor industry.

Our research network brings together six leading Irish universities: Tyndall National Institute, University College Dublin, Munster Technological University, South East Technological University Carlow, University of Limerick and Maynooth University. These collaborative academic teams work closely with industry to drive innovation and support the continued growth of the semiconductor sector.

As a recognised centre for excellence in microelectronic integrated circuit design, MCCI focuses on advanced analog, mixed-signal, RF, and sub millimeter-wave technologies. Based at Tyndall National Institute in Cork, we operate within a dynamic ICT research environment supported by Enterprise Ireland and a broad base of industry partners. Our strategic position enables close collaboration with expert groups in areas such as magnetics, photonics, nanomaterials and quantum technologies, facilitating the development of real world applications.

Working alongside global semiconductor companies, our research teams produce system-level demonstrators and prototypes that address key technological challenges. These partnerships help ensure our work remains relevant and aligned with evolving industry needs.

One of the most tangible indicators of our impact is the successful transition of MCCI researchers and PhD graduates into technical leadership roles across Ireland's semiconductor ecosystem. We remain committed to educating and mentoring the next generation of microelectronics engineers and innovators.

Through our collaborative, industry-focused approach, MCCI continues to deliver meaningful results, contributing to peer-reviewed publications, advanced technology platforms, and a pipeline of intellectual property. We provide academic partners with access to advanced design tools, methodologies, and infrastructure, as well as support for wafer fabrication and packaging through leading foundries.

Our capabilities have recently expanded with the establishment of a Cryogenic Lab and a high voltage power lab in Tyndall. Enabling integrated circuit testing at temperatures as low as 4 Kelvin and high voltage measurement capability for power management. These facilities strengthens our pioneering work in Cryogenic-CMOS research and opens new opportunities for innovation.

Guided by a technical steering panel of academic and industry experts, MCCI's research aligns with global technology roadmaps. The outcomes of our work contribute directly to the creation and growth of startups and SMEs across a range of sectors, including wireless communications, Industry 5.0, biomedical devices, and IoT applications for homes, industry and agriculture.

Our research teams are based across six of Ireland's universities; Tyndall National Institute, University College Dublin, Munster Technological University, SETU Carlow, University of Limerick and Maynooth University and they work with many industry partners on technological advances for the growth of the semiconductor sector.

1 Tyndall National Institute Institiúid Náisiúnta

2 MTU Ollscoil Teicneolaíochta na Mumhan Munster Technological University

3 University of Limerick Ollscoil Luimnigh

4 SETU Ollscoil Teicneolaíochta an Oirdheiscirt South East Technological University

5 Maynooth University National University of Ireland Maynooth

6 University College Dublin Ireland's Global University

MCCI Teams

Tyndall National Institute

- Vishal Japtap Head of Group
- Hugo Cruz Principle Investigator
- Prof. Pádraig Cantillon-Murphy, Principle Investigator (BioMedical Imaging)
- Dr. John Buckley, Principle Investigator (RF Wireless Antenna & Systems)
- Dr. Daniel O'Hare, Principle Investigator (Sensor Interfaces & Precision Circuits)
- Prof. Dimitra Psychogiou, Principle Investigator (RF & mm wave)
- Mr Seamus O'Driscoll, Principle Investigator of Power Management (ULP PMIC)
- Dr. Gerardo Salgado, Senior Researcher
- Subhash Chevella Senior Researcher
- Anita Schuler, Senior Digital Design Engineer
- Shane O'Neill, Senior IC Layout Design Engineer

University College Dublin

- Prof. Peter Kennedy, Principle Investigator (RF PLL/Freq Generation)
- Prof. R. Bogdan Staszewski, PI, (RF Freq Gen & RF Transceivers)
- Prof. Anding Zhu, PI, (RF & mmw Transceivers)
- Dr. Teerachot Siriburanon, PI, (RF)
- Dr. Elena Blokhina, PI, Quantum and device models
- Dr. Deepu John, PI, Edge AI
- Dr. Barry Cardiff, Calibration and AI

University of Limerick

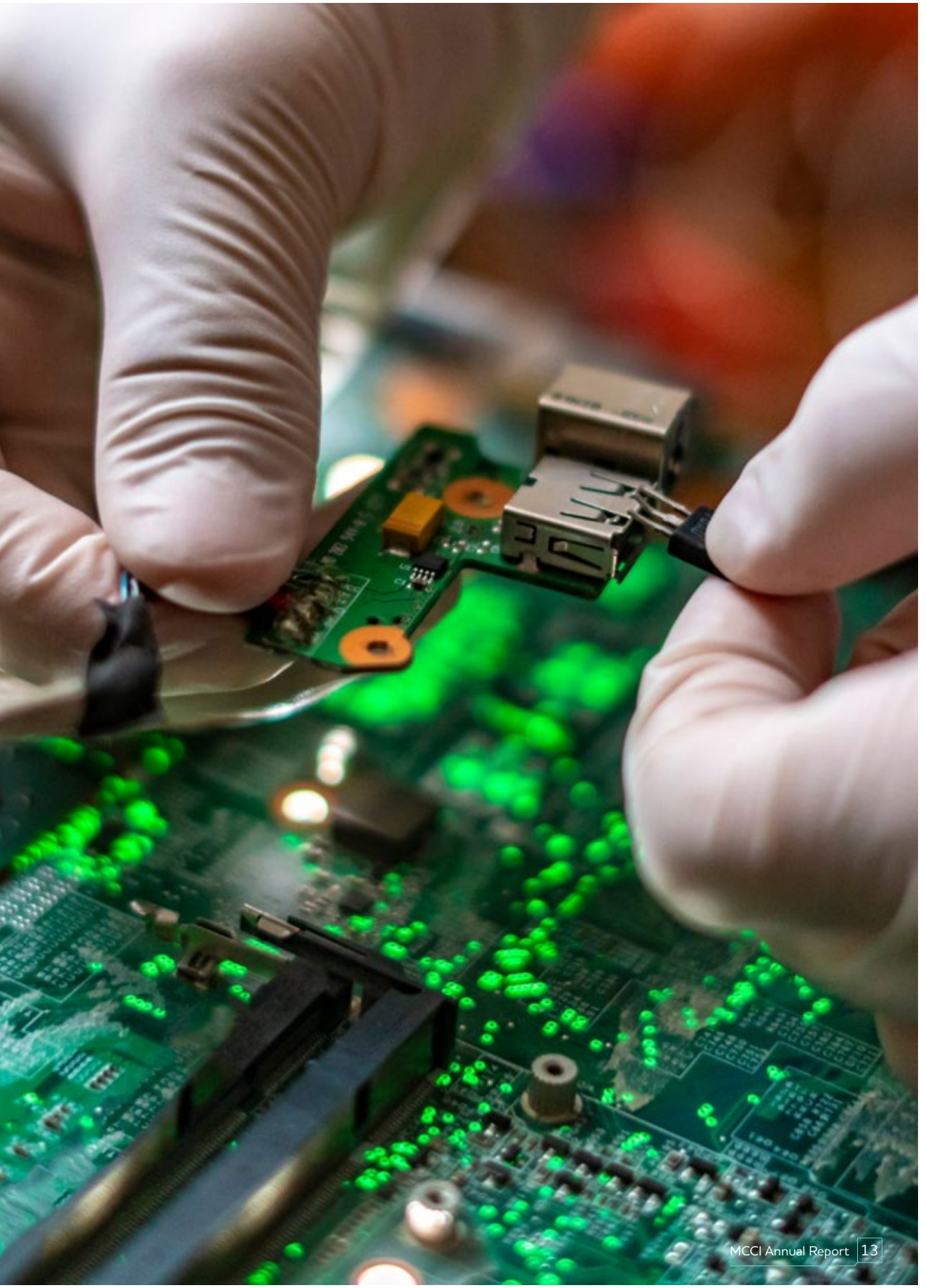
- Dr Brendan Mullane, Principle Investigator (Digital Signal Processing (DSP) and CPU)

South East Technological University

- Dr Darren Francis Kavanagh, Principle Investigator (Analog Mixed-Signal Design)
- Dr Vincent O Brien, Principle Investigator (Analog Mixed-Signal Design)

Maynooth University

- Dr. John Dooley
- Johnathan Guimaraes Ribeiro



Research Pillars

Research Pillars

Broadband & Low Power RF Transceivers

Our RF & mm wave research is focused on for next generation low power broadband data-centres and cloud computing. RF for next generation wireless 5/6G communications, medical, environmental sensing, imaging and stimulation.

Power Management

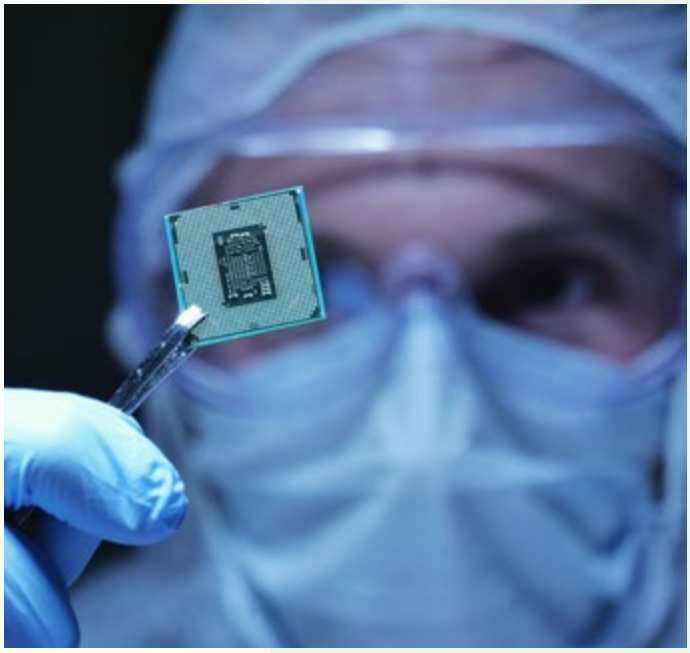
This strategy is focused on Ultra Low Power (ULP) and higher efficiency PMIC integrated systems, and energy harvesting solutions. Research is exploring highly integrated power supplies systems to address the need for smaller physical form factors and energy reduction while achieving higher energy efficiency challenges.

RF to sub millimeter Wave

Our RF to sub millimeter wave research is focused on applications of microwave and millimetre wave RF front-end components, RF co-design methods for multi-functional , millimeter and sub millimeter wave. RF components, filter synthesis techniques, broadband antenna arrays and low-cost integration methods for wireless, imaging space and defence communication systems.

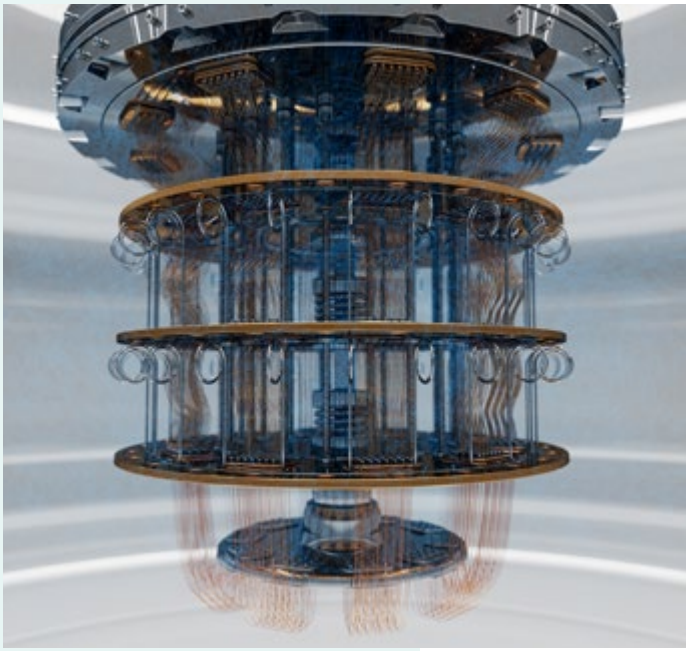
Precision Analog Circuits

Our Precision Analog Circuits research explores ultra-low power high dynamic range data converters, multi-sensor interfaces, analogue front ends for ultra-low power applications in Industrial 4.0 and Biomedical/Medical devices including implantables.



The Intelligent Edge & Digital

We are exploring new lower power efficient circuit architectures for data sensing, measurement & data conversion to digital and stored incorporating Machine learning (ML) and AI. Data Security is a growing concern globally and research investigations into how circuit design partitioning can help achieve a more secure data network.



Cryongenic CMOS Controllers for Quantum

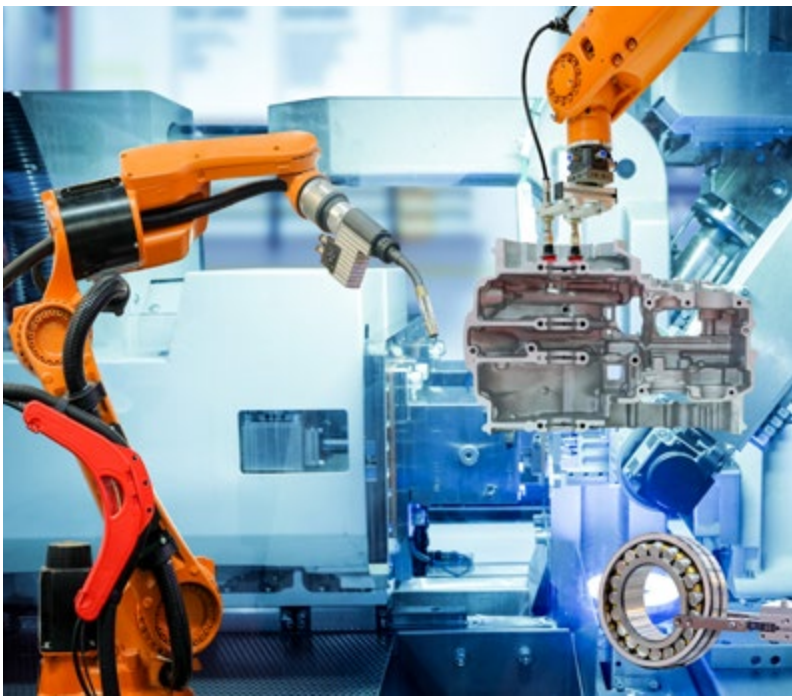
A new research pillar, Cryogenic CMOS will examine and develop CMOS circuit designs that operate effectively at ultralow temperatures, i.e. down to 4 degree Kelvin. Part of the research is investigating how PCB testing materials and spice level models for circuit design behave at these temperatures and verify new methods and techniques for improved performance.

Application Areas

BioMedical & Medtech

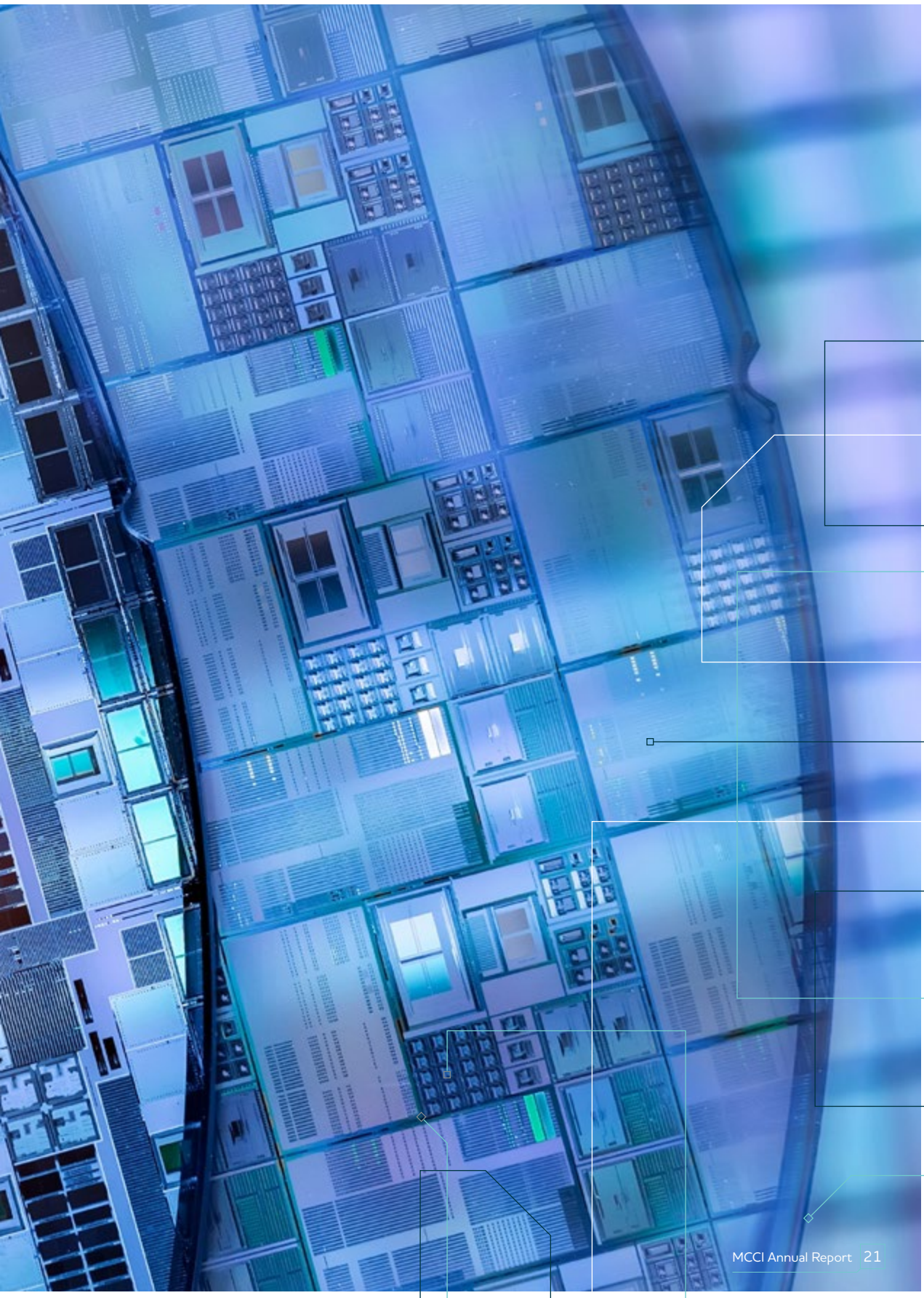
Power Management & Energy

Wireless Communications



Industrial, Instrumentation & IOT

MCCI Industry Members



Research Leadership Team

Research Leaders

Dr. Vishal Japtap

Dr. Hugo Cruz

Dr. Danny O'Hare

Dr. Gerardo Salgado

Dr. John Buckley

Prof. R. Bogdan Staszewski

Dr. Teerachot Siriburanon

Dr. Deepu John

Dr. Pádraig Cantillon-Murphy

Dr. Brendan Mullane

Prof. Dimitra Psychogiou

Prof. Peter Kennedy

Prof. Anding Zhu

Dr. Elena Blokhina

Mr. Seamus O'Driscoll

Dr. Barry Cardiff

Dr. Darren Francis Kavanagh

2024 Highlights

A major highlight was the acceptance of a paper by Prof. Michael Peter Kennedy and Valerio Mazzaro at ISSCC 2024

A fantastic achievement for Prof. Kennedy, UCD researchers, and the MCCI team. The ground-breaking work, carried out in close collaboration with the ADI Limerick RF team, resulted in the paper "A 45.5fs Integrated Random Jitter and 75dBc Integer Boundary Spur BiCMOS Fractional PLL with Suppression of Fractional, Horn and Wandering Spur." Prof. Kennedy presented the paper at the conference in February 2024.

In 2024, MCCI made two significant strategic appointments to strengthen its research leadership and expand its expertise.

Dr. Vishal Jagtap was appointed Head of Group. He joined MCCI from the Institute for High-Frequency and Communication Technology at the University of Wuppertal, Germany. With a strong background in high-frequency systems and research leadership, Dr. Jagtap brings valuable insights and a fresh strategic perspective to the team. He will lead MCCI's new research initiative on silicon-integrated terahertz (THz) transceivers for imaging applications.

Dr. Hugo Cruz joined as Principal Investigator in the Integrated Power Systems group. His research focuses on low-power energy harvesting Power Management Integrated Circuits (PMICs) and granular Point-of-Load (PoL) Integrated Voltage Regulators (iVRs). His expertise further enhances MCCI's capabilities in power management solutions, opening new avenues for industry collaboration in developing next-generation energy-efficient systems.

▲ Dr. Vishal Jagtap

▲ Dr. Hugo Cruz

▲ L to R John Morrissey MCCI, Prof. Bogdan Staszewski UCD, Yevhenii Mormui UCD, Philip Quinlan Analog Devices & Dr. Viet Nguyen UCD

Student Recognition

MCCI Master's research student Yevhenii Mormul was awarded the Analog Devices (ADI) Outstanding Student IC Designer Award for 2024 (EU Region). This prestigious award recognises his outstanding work on a Time-to-Digital Converter (TDC) for cryogenic applications implemented in 28nm CMOS technology—an important milestone in both his academic career and MCCI's ongoing research excellence.

Knowledge Exchange and Thought Leadership

The MCCI IEEE Distinguished Lecturer Series continued in 2024, featuring high-profile speakers.

Dr. Alvin Loke's IEEE SSCS Society Lecture on "Extending and Augmenting Analog with Digital to Overcome Technology Scaling Limitations" took place on 17th May.

Hardware Security and Safety of IC Chips and Systems, was held on 29th October with Prof. Makoto Nagata

Prof. Makoto Ikeda, The University of Tokyo, Japan presented "Acceleration of Encryption Algorithms, Elliptic Curve, Pairing, Post Quantum Cryptoalgorithm (PQC), and Fully Homomorphic Encryption (FHE)"

▲Dr. Alvin Loke (Intel, USA)

▲Prof. Makoto Nagata (Kobe University, Japan)

▲Prof. Makoto Ikeda (The University of Tokyo, Japan)

MCCI Attend IEEE Biomedical Circuits and Systems Conference – BioCAS in Xi'an, China

Researchers from MCCI participated in the IEEE Biomedical Circuits and Systems Conference (BioCAS) 2024, held in Xi'an, China. The conference is a leading international venue for the presentation of research in biomedical circuits and systems, with a focus on innovation in healthcare technologies.

MCCI team members Danny O'Hare, Cian O'Donnell, Zhongzheng Wang, Manish Srivastava, and Javier Higes Marquez attended the conference and contributed two technical papers showcasing recent developments in bio-sensing and analog design methodologies. MCCI had 2 papers accepted at the conference.

1. **Fast Square Wave-based Electrochemical Impedance Spectroscopy for Impedance-based Biomedical Applications** Authors: Zhongzheng Wang, Han Shao, Alan O'Riordan, Javier Higes-Marquez, Ivan O'Connell, and Daniel O'Hare
2. **Efficient Bio-Sensing Amplifier Design: A Python-Based gm/ID Design Methodology** Authors: Manish Srivastava, Cian O'Donnell, Ben Griffin, Padraig Cantillon-Murphy, and Daniel O'Hare

MCCI Presents Mixed-Signal Research at IEEE ICECS 2024 in France

MCCI researchers participated in the IEEE International Conference on Electronics, Circuits and Systems (ICECS) 2024, held in Nancy, France. ICECS is a key conference in the IEEE Circuits and Systems Society calendar, focusing on the latest advances in analog, digital, and mixed-signal circuits and systems.

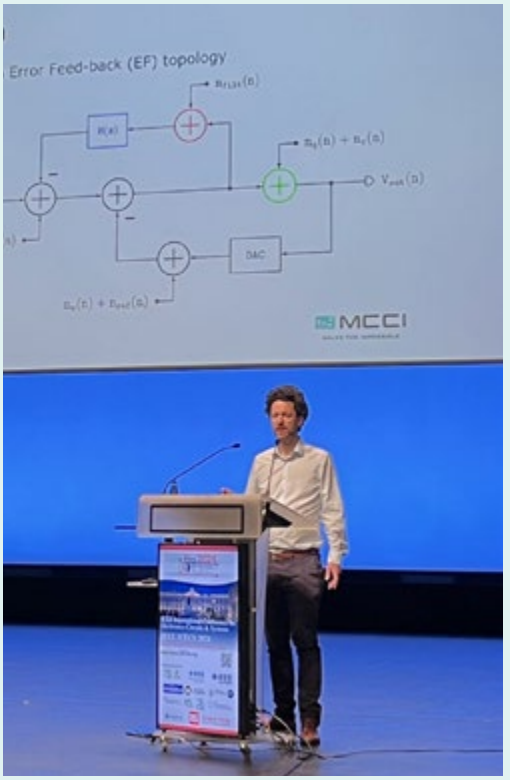
Congratulations to Danny O'Hare and the team, who presented two papers highlighting recent developments in data converter design and low-power circuit techniques.

1. A Digitally Calibrated 1st Order Noise-Shaped SAR ADC in 28 nm CMOS

Authors: Subhash Chevella, Gerardo Molina Salgado, Armia S., Anita Schuler, Barry Cardiff, Ivan O'Connell, and Danny O'Hare

2. A Counting-Based Bridge-to-Digital Converter Achieving a Walden FoM of 0.048 nJ/conv-step

Authors: Annamaria Fordymacka, Gerardo Molina Salgado; Ivan O'Connell



European Chips JC Collaboration

MCCI was a key consortium partner with Tyndall, MIDAS Ireland and UCD/NOVA in a successful proposal to the EU Chips Joint Undertaking. Their submission for establishing the "IC-3" Irish Competency Centre was approved for funding by both the EU and Ireland's Department of Enterprise, Trade and Employment (DETE). IC-3 is scheduled to launch in 2025, enhancing Ireland's strategic capabilities in semiconductor R&D.

I-C3

MCCI Technical Conference (MTC) 2024

In June, MCCI hosted its annual MCCI Technical Conference (MTC) at Tyndall National Institute, welcoming over 90 industry and academic members to a full day of technical presentations, networking and knowledge exchange.

The conference featured six thematic sessions, where members of the MCCI research team presented updates and insights across a broad range of microelectronics research areas:

- ADC Architectures
- ADCs & Power-Efficient Design
- Biomedical Circuits & Systems
- RF Technologies
- Modelling & Cryogenic Circuits
- RF & Optical Integration

Alongside the technical sessions, the day also included a lively poster session, with 20 posters showcasing the work of postgraduate researchers. The session provided a platform for emerging talent to engage with attendees and discuss ongoing research. Congratulations to all students and their supervisors for their strong contributions. MTC is an exclusive member event, designed to provide early access to emerging research directions across MCCI's program areas. It continues to serve as a valuable opportunity for collaboration, discussion, and community building within Ireland's microelectronics ecosystem.

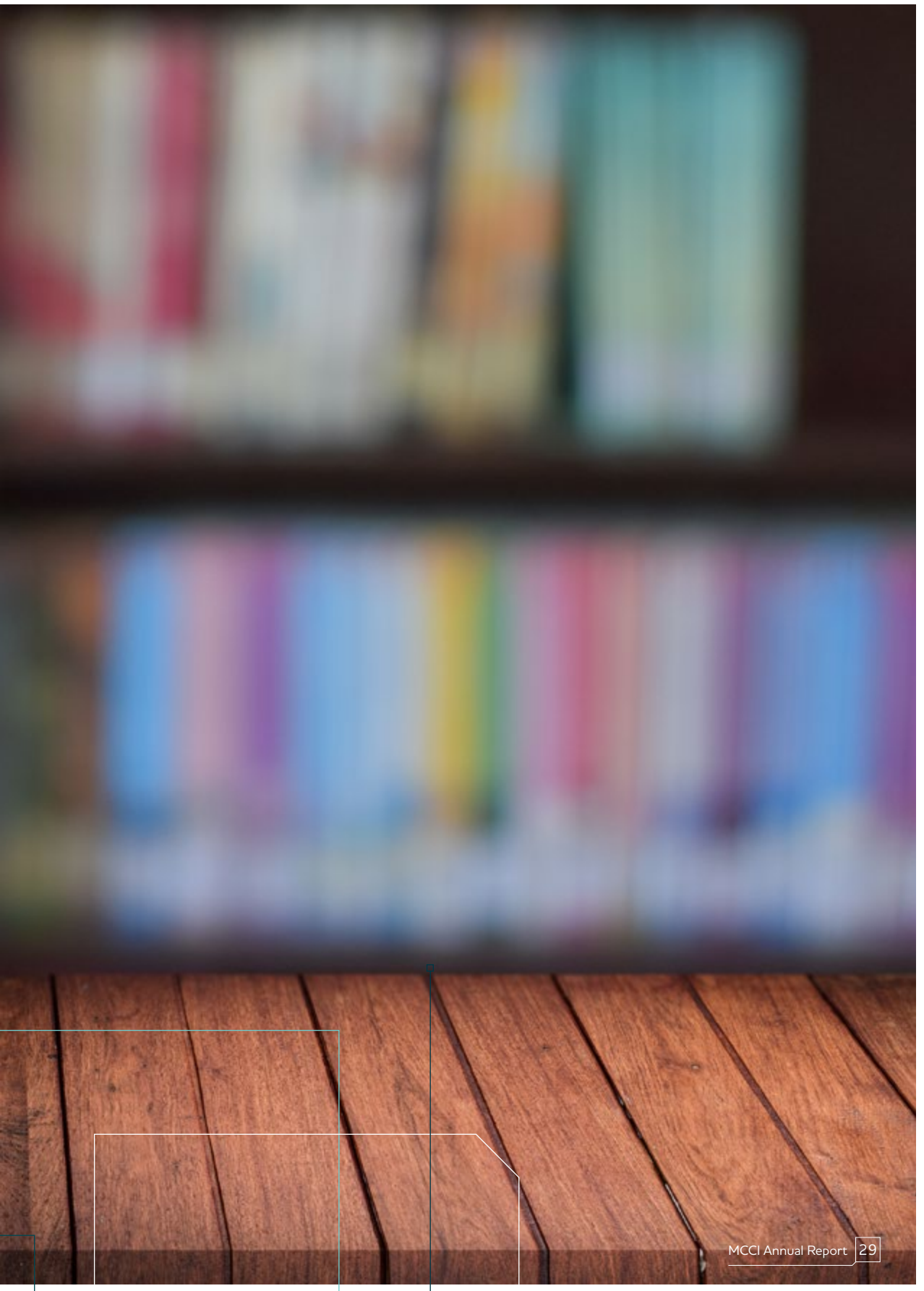
IEEE International Midwest Symposium

In August, MCCI researchers attended the IEEE International Symposium on Circuits and Systems (MWSCAS) 2024, held in Springfield, Massachusetts, USA. The event provided a forum for sharing ongoing research across a wide range of circuit and system design topics.

MCCI team members Gerardo M. Salgado, Mauricio Montanares, Victor Arzate, and Minda Minda Wen participated in a session focused on Cryogenic CMOS Circuits for Quantum Computing Applications.

Mauricio Montanares, Minda Minda Wen, and Victor Arzate each presented papers related to their current work on cryo-CMOS technologies.

Research Publications



Tier One Publications

1. **M.P. Kennedy, V. Mazzaro, S. Tulisi, M. Scully, N. McDermott, J. Breslin.** "A 45.5fs-Integrated-Random-Jitter and -75dBc Integer Boundary Spur BiCMOS Fractional-N PLL with Suppression of Fractional, Horn and Wandering Spurs", **ISSCC,** Feb 2024
2. **M. Srivastava, A. Ferro, A, Sidun, J. De La Rosa, K. O'Donoghue, P. Cantillon-Murphy, D. O'Hare,** "A Small-Area 2nd-Order Adder-Less Continuous-Time ΔΣ Modulator With Pulse Shaping FIR DAC for Magnetic Sensing", **OJ-CAS,** Mar 2024
3. **A. Wall, P. Walsh. D. O'Hare,** "A Model & Design Methodology for Dead Time Linearised Current Controlled Ring Oscillator ADCs", **TCAS-II, Apr 2024**
4. **M. Srivastava, K. O'Donoghue, A, Sidun, H. A. Jaeger, A. Ferro, D. Crowley, C. van den Bosch, M. Kennedy, D. O'Hare, P. Cantillon-Murphy,** "3D Position Tracking using On-chip Magnetic Sensing in Image-guided Navigation Bronchoscopy", **TBioCAS,** Apr 2024
5. **Steele, D. Psychogiou,** "Wideband Broadside-Coupled Line Baluns Enabled by Multimaterial Additive Manufacturing", **MTT,** May 2024
6. **D. Rivera-Orozco, F. Sandoval-Ibarra, G. Salgado,** "On the Application of Data Weighted Averaging to Noise Shaping SAR ADCs", **ISCAS,** May 2024
7. **M. Venkatesh, G. Salgado, K. McCarthy, I. O'Connell** "A Low Power Programmable Switch Supply Dynamic Comparator", **ISCAS,** May 2024
8. **S. Kumar, P. Sawakewang, T. Siriburanon, R. B. Staszewski ,** "A 25.4-27.5 GHz Ping-Pong Charge-Sharing Locking PLL Achieving 42 fs Jitter with Implicit Reference Frequency Doubling", **VLSI,** June 2024
9. **G. Wang, Q. Wang, G. Iyer, A. Nag, D. John**, "Unsupervised Pre-Training Using Masked Autoencoders for ECG Analysis", **BioCAS,** Oct 2023
10. **M. Venkatesh, G. M. Salgado, K. McCarthy, I. O'Connell,** "A 500 kS/s 71.8 dB 5.7 fJ/Conv-step Switch Supply Based Comparator SAR ADC for Biomedical Portable Devices", **BioCAS,** Oct 2023
11. **H. Yin, A. Zhu,** "Iterative Multimetric Model Extraction for Digital Predistortion of RF Power Amplifiers Using Enhanced Quadratic SPSA", **MTT,** Sep 2023
12. **Q. Luo, A. Zhu,** "Widen Linearization Angle of Beamforming Arrays With Semi-Partitioned Digital Predistortion", **IMS** Jun 2023
13. **D. Psychogiou, K. Zhao,** "High-Q Monolithically-Integrated Bandpass Filters Using Quarter-Spherical Resonators", **IMS** Jun 2023
14. **Z. Zhang, D. Psychogiou,** "Multi-configurable Bandpass Filters with Tune-all Single-, Dual-band Transfer Functions and Reconfigurable Directionality", **IMS** Jun 2023
15. **K. Zhao, D. Psychogiou,** "Compact 3D-Printed Bandpass Filters Using Coaxial and Dual-mode Ridged-Waveguide Resonators", **IMS** Jun 2023
16. **D. Mai, M. P. Kennedy,** "Initial Condition-Dependent Spur Pattern Induced by Undithered MASH DDSM Divider Controller", **ISCAS** May 2023
17. **X. Chen, Y. Hu, T. Siriburanon, J. Du, R. B. Staszewski, A, Zhu,** "A 30-GHz Class-F Quadrature DCO Using Phase Shifts between Drain–Gate–Source for Low Flicker Phase Noise and I/Q Exactness", **JSSC,** Jan 2023.
18. **Y. Kandeel, S. O'Driscoll, C. O'Mathuna, M. Duffy,** "Optimum Phase Count in a 5.4-W Multiphase Buck Converter Based on Output Filter Component Energies", **TPEL,** Dec 2022
19. **C. Chu, J. Pang,A. Zhu,** "Broadband Sequential Load Modulated Balanced Amplifier With Extended Design Space Using Second Harmonic Manipulation", **MTT,** Dec 2022
20. **C. Chu, V. Tamrakar,... A. Zhu,** "High-Efficiency Class-iF-1 Power Amplifier With Enhanced Linearity", **MTT,** Dec 2022
21. **R. B. Staszewski, A. Esmailiyan, H. Wang, E. Koskin, P. Giounanlis, X. Wu, A. Koziol, A. Sokolov, I. Bashir, M. Asker, D. Leipold, R. Nikandish, T. Siriburanon and E. Blokhina,** "Cryogenic Controller for Electrostatically Controlled Quantum Dots in 22-nm Quantum SoC", **OJ-SSCS,** Oct. 2022.

22. **T. Kobal, A. Zhu,** "Digital Predistortion of RF Power Amplifiers With Decomposed Vector Rotation-Based Recurrent Neural Networks", **MTT,** Oct 2022

23. **M. Saeed, O. Märtens, B. Larras, A. Frappé, D. John, B. Cardiff,** "Event-Driven ECG Classification using Functional Approximation and Chebyshev Polynomials", **BioCAS,** Oct 2022

24. **C. O'Mathúna, S. O'Driscoll,** "Heterogeneous Integration of Power Conversion using Power Supply on Chip and Power Supply in Package", **Focus Topic / Invited Lecture, EPE ECCE,** Sep 2022

25. **Bozorg A, Staszewski R B,** "A Charge-Sharing IIR Filter With Linear Interpolation and High Stopband Rejection", **JSSC,** May 2022

26. **A. Wall, P. Walsh, K. Sadeghipour, I. O'Connell, D. O'Hare,** "An Improved Linearity Ring Oscillator-Based Current-to-Digital Converter", **SSC-L,** Aug 2022

27. **X. Chen, T. Siriburanon, Z. Wang, J. Du, Y. Hu, A. Zhu, R. B. Staszewski,** "A Digital-to-Time Converter Based on Crystal Oscillator Waveform Achieving 86-fs Jitter in 22-nm FD-SOI CMOS", **RFIC,** June 2022

28. **A. Bozorg and R. B. Staszewski,** "A Charge-Rotating IIR Filter with Linear Interpolation and High Stop-Band Rejection", **JSSC,** May 2022

29. **T. Kobal, Y. Li, X. Wang, A. Zhu**, "Digital Predistortion of RF Power Amplifiers With Phase-Gated Recurrent Neural Networks", **MTT,** April 2022

30. **Mai D, Donnelly Y, Kennedy MP, Tulisi S, Breslin J, Griffin P, Connor M, Brookes S, Shelly B, Keaveney M,** "Wandering Spur Suppression in a 4.9-GHz Fractional-N Frequency Synthesizer", **JSSC,** Apr 2022

31. **X. Wang, Y. Li, A. Zhu,** "Digital Predistortion Using Extended Magnitude-Selective Affine Functions for 5G Handset Power Amplifiers With Load Mismatch", **MTT,** Mar 2022

32. **J. Pang, C. Chu, J. Wu, Z. Dai, M. Li, S. He, A. Zhu,** "Broadband GaN MMIC Doherty Power Amplifier Using Continuous-Mode Combining for 5G Sub-6 GHz Applications", **JSSC,** Feb 2022

33. **C. Chu,.... A. Zhu,** "Waveform Engineered Sequential Load Modulated Balanced Amplifier With Continuous Class-F–1 and Class-J Operation", **MTT,** Feb 2022

34. **H. M. Nguyen, J. S. Walling, A. Zhu, R. B. Staszewski,** "A mm-Wave Switched-Capacitor RFDAC", **JSSC,** Feb 2022

35. **G. Sivapalan, K. Nundy, S. Dev, B. Cardiff, D. John**, "ANNet: A Lightweight Neural Network for ECG Anomaly Detection in IoT Edge Sensors", **TBioCAS,** Jan 2022

36. **X. Wang, Y. Li, H. Yin, C. Yu, Z. Yu, W. Hong, A. Zhu,** "Digital Predistortion of 5G Multiuser MIMO Transmitters Using Low-Dimensional Feature-Based Model Generation", **MTT,** Dec 2021

37. **Y. Li, X. Wang, A. Zhu,** "Reducing Power Consumption of Digital Predistortion for RF Power Amplifiers Using Real-Time Model Switching", **MTT**, Dec 2021

38. **M. Saeed, Q. Wang,... B. Cardiff, D. John,** "Evaluation of Level-Crossing ADCs for Event-Driven ECG Classification", **TBioCAS**, Dec 2021

39. **A. John, K. Nundy, B. Cardiff, and D. John,** "Multimodal Multiresolution Data Fusion Using Convolutional Neural Networks for IoT Wearable Sensing", **TBioCAS,** Dec 2021

40. **S. Dartizio,... L. Avallone,... M. P. Kennedy,.. S. Levantino,** "A 12.9-to-15.1GHz Digital PLL Based on a Bang-Bang Phase Detector with Adaptively Optimized Noise Shaping Achieving 107.6fs Integrated Jitter", **JSSC,** Oct 2021

41. **J. Du, T. Siriburanon, X. Chen, Y. Hu, V. Govindaraj, A. Zhu, R. B. Staszewski,** "A Millimeter-Wave ADPLL With Reference Oversampling and Third-Harmonic Extraction Featuring High FoMjitter-N", **SSC-L,** Oct 2021

42. **V. Nguyen, F. Schembari, R. B. Staszewski,** "A Deep-Subthreshold Variation-Aware 0.2-V Open-Loop VCO-Based ADC", **JSSC,** Oct 2021

43. **Li Y, Wang X, Pang J, Zhu A,** "Boosted Model Tree-Based Behavioral Modeling for Digital Predistortion of RF Power Amplifiers", **MTT,** Sep 2021

44. **Y. Hu, X. Chen, T. Siriburanon, J. Du, V. Govindaraj, A. Zhu and R. B. Staszewski,** "A Charge-Sharing Locking Technique With a General Phase Noise Theory of Injection Locking". **JSSC,** Sep 2021

45. **D. Mai, Y. Donnelly, M. P. Kennedy, S. Tulisi, J. Breslin, P. Griffin, M. Connor, S. Brookes, B. Shelly and M. Keaveney,** "Experimental Verification of Wandering Spur Suppression Technique in a 4.9GHz Fractional-N Frequency Synthesizer", **ESSCIRC,** Sept 2021

46. **A. Bozorg and R. B. Staszewski,** "A Charge-Rotating IIR Filter with Linear Interpolation and High Stop-Band Rejection", **ESSCIRC,** Sept 2021

47. **E. Kobal, T. Siriburanon, R. B. Staszewski and A. Zhu,** "A 28 GHz Switched-Filter Phase Shifter with Fine Phase-Tuning Capability Using Back-Gate Biasing in 22 nm FD-SOI CMOS", **ESSCIRC**, Sept 2021

48. **J. Du, T. Siriburanon, Y. Hu, V. Govindaraj and R. B. Staszewski,** "A Reference-Waveform Oversampling Technique in a Fractional-N ADPLL," **JSSC,** Aug 2021

49. **J. Du, Y. Hu, T. Siriburanon, E. Kobal, P. Quinlan, A. Zhu and R. B. Staszewski,** "A Compact 0.2–0.3-V Inverse-Class-F23 Oscillator for Low 1/f3 Noise over Wide Tuning Range," **JSSC,** Aug 2021

50. **Q. Luo, ...X. Wang, C. Chu, A. Zhu,** " Linearization Angle Widened Digital Predistortion for 5G MIMO Beamforming Transmitters", **MTT,** July 2021

51. **A. Bozorg and R. B. Staszewski,** "A clock-phase reuse technique for discrete-time band-pass filters," **JSSC,** June 2021

52. **J. Du, T. Siriburanon, X. Chen, Y. Hu, V. Govindaraj, A. Zhu and R. B. Staszewski,** "A 24-31 GHz Reference Oversampling ADPLL Achieving FoMjitter-N of -269.3 dB", **VLSI,** June 2021

53. **P. Chen, F. Zhang, S. Hu and R. B. Staszewski,** "A Feedforward and Feedback Constant-Slope Digital-to-Time Converter in 28nm CMOS Achieving ≤ 0.12% INL/ Range over >100mV Supply Range", **VLSI,** June 2021

54. **H. M. Nguyen, J. S. Walling, A. Zhu, R. B. Staszewski**, "A Ka-Band Switched-Capacitor RFDAC Using Edge-Combining in 22nm FD-SOI", **VLSI,** June 2021

55. **R. B. Staszewski,** "Quantum Computer on a Chip," Workshop (1-hr), WSE-8, "Cryogenic Electronics for Quantum Computing and Beyond: Applications, Devices, and Circuits", **RFIC,** June 2021

56. **A. John, B. Cardiff, D. John,** "A 1D-CNN Based Deep Learning Technique for Sleep Apnea Detection in IoT Sensors", **ISCAS,** May 2021

57. **M. Saeed, Q. Wang, O. Märtens, B. Larras, A. Frappé, B. Cardiff, D. John,** "Event-Driven ECG Classification Using an Open-Source, LC-ADC Based Non-Uniformly Sampled Dataset", **ISCAS,** May 2021

58. **C. Smyth, G. Wang, R. Panicker, A. Nag, B. Cardiff, D. John,** "Continuous User Authentication Using IoT Wearable Sensors", **ISCAS,** May 2021

59. **Li Y, Wang X, Zhu A,** "Complexity-Reduced Model Adaptation for Digital Predistortion of RF Power Amplifiers with Pretraining-Based Feature Extraction", **MTT,** Mar 2021

60. **Y Xu, J Pang, X Wang, A Zhu,** "Three-Stage Load Modulated Power Amplifier With Efficiency Enhancement at Power Back-Off", **MTT,** Mar 2021

61. **Yang Xu, Jingzhou Pang, Xiaoyu Wang, Anding Zhu,** "Enhancing bandwidth and back-off range of Doherty power amplifier with modified load modulation network", **MTT,** Feb 2021

62. **M. Mercandelli,... L. Avallone,... M. P. Kennedy,.. S. Levantino,** "A 12.9-to-15.1GHz Digital PLL Based on a Bang-Bang Phase Detector with Adaptively Optimized Noise Shaping Achieving 107.6fs Integrated Jitter", **ISSCC,** Feb 2021

63. **A. Santicciolli,... L. Avallone,... M. P. Kennedy,.. S. Levantino,** "A 98.4fs-Jitter 12.9-to-15.1GHz PLL-Based LO Phase-Shifting System with Digital Background Phase-Offset Correction for Integrated Phased Arrays", **ISSCC,** Feb 2021

64. **A. Bozorg and R. B. Staszewski,** "A 0.02–4.5 GHz LN(T) A in 28-nm CMOS for 5G exploiting noise reduction and current reuse," **JSSC,** Feb. 2021

65. **G. Nikandish, R. B. Staszewski and A. Zhu,** "Unbalanced power amplifier: An architecture for broadband back-off efficiency enhancement," **JSSC,** Feb. 2021

66. **R. B. Staszewski, P. Giounanlis, A. Esmailiyan, H. Wang, I. Bashir, C. Cetintepe, D. Andrade-Miceli, M. Asker, D. Leipold, T. Siriburanon, A. Sokolov and E. Blokhina,** "Position-based CMOS charge qubits for scalable quantum processors at 4K", **ISCAS,** Oct. 2020

67. **P. Giounanlis, A. Sokolov, E. Blokhina, I. Bashir, D. Leipold and R. B. Staszewski,** "Electrostatic control and entanglement of CMOS position-based qubits," **ISCAS,** Oct. 2020

68. **S. Binsfeld-Ferreira and R. B. Staszewski,** "Design of Ultra-Low-Power Discrete-time Receivers for the Internet of Things", Mini- tutorial (2-hrs), MT-3b, **ISCAS,** Oct. 2020

69. A**. Bozorg, R. B. Staszewski,** "A 0.02-4.5-GHz LN(T)A in 28-nm CMOS for 5G Exploiting Noise Reduction and Current Reuse", **JSSC,** Sep 2020.

70. **R. B. Staszewski, Y. Hu, and T. Siriburanon,** "Digital PLLs for Millimeter Wave – A Tutorial," Workshop (1.5-hr) presented at Virtual Educational Workshop 4: New 5G integration solutions, and related technologies, **ESSCIRC,** Sept. 2020

71. **A. Esmailiyan, H. Wang, M. Asker, E. Koskin, D. Leipold, I. Bashir, K. Xu, A. Koziol, E. Blokhina, and R. B. Staszewski,** "A fully integrated DAC for CMOS position-based charge qubits with single-electron detector loopback testing", **SSC-L,** Aug 2020

72. **Chevella, S, O'Hare, D and O'Connell, I.,** "A Low-Power 1-V Supply Dynamic Comparator", **SSC-L,** July 2020

73. **X. Chen, Y. Hu, T. Siriburanon, J. Du, R. B. Staszewski, and A. Zhu,** "A tiny complementary oscillator with noise reduction using a triple-8-shaped transformer", **SSC-L,** July 2020

74. **J. Du, T. Siriburanon, Y. Hu, V. Govindaraj, and R. B. Staszewski,** "A 2.0–2.87GHz -249dB FoM 1.1 mW digital PLL exploiting reference-sampling phase detector", **SSC-L,** July 2020

75. **A. Fordymacka et al,** "A 0.01mm2 0.83V Input Range SAR Based Bridge-to-Digital Converter", SSC-L, 2020

76. **G. M. Salgado, D. O'Hare, and I. O'Connell,** "Modeling and Analysis of Error Feedback Noise-Shaping SAR ADCs", **ISCAS,** May 2020

77. **A. John, B. Cardiff, D. John,** "A Generalized Signal Quality Estimation Method for IoT Sensors", **ISCAS**, May 2020

78. **S. Hu, J. Du, P. Chen, H. M. Nguyen, P. Quinlan, B. Staszewski,** "A Type-II Phase-Tracking Receiver", **(JSSC),** July 2020

79. **R. B. Staszewski,** "Beyond All-Digital PLL for RF and Millimeter-Wave Frequency Synthesis," Workshop presentation (1.5-hr) at Educational Session 2: Phase-Locked Loops, **CICC,** Mar. 2020

80. **Y. Hu, X. Chen, T. Siriburanon, J. Du, Z. Gao, V. Govindaraj, A. Zhu, R. B. Staszewski,** "A 21.7-26.5GHz Charge-Sharing Locking Quadrature PLL with Implicit Digital Frequency Tracking Loop Achieving 75fs Jitter and -250dB FoM", **(ISSCC)**,

81. **H. Wang, F. Schembari, and R. B. Staszewski,** "An event-driven quasi-level-crossing delta modulator based on residue quantization," **(JSSC),** Nov 2019

82. **Chen P, Zhang F, Zong Z, Hu S, Siriburanon T, Staszewski RB,** "A 31-μ W, 148-fs Step, 9-bit Capacitor-DAC-Based Constant-Slope Digital-to-Time Converter in 28-nm CMOS", **(JSSC),** Nov 2019

83. **Li M, Pang J, Li Y, Zhu A,** "Ultra-Wideband Dual-Mode Doherty Power Amplifier Using Reciprocal Gate Bias for 5G Applications", **(MTT)** Oct 2019

84. **M.P. Kennedy, Y. Donnelly, J. Breslin, S. Tulisi, S. Brookes, S. Patil, C. Curtin, B. Shelly, P. Griffin and M. Keaveney,** "4.48GHz 180nm SiGe BiCMOS Fractional-N Frequency Synthesizer with Spurious-Tone Suppression via Probability Mass Redistribution", **(SSC-L),** Sep 2019

85. **G. Nikandish, R. B. Staszewski, and A. Zhu,** "Broadband fully integrated GaN power amplifier with embedded minimum inductor bandpass filter and AM-PM compensation,", **(ESSCIRC),** Sep 2019

86. **Y. Donnelly, M. P. Kennedy, J. Breslin, S. Tulisi, S.Patil, C. Curtin, S. Brookes, B. Shelly, P. Griffin, M. Keaveney,** "4.48-GHz Fractional- N Frequency Synthesizer With Spurious-Tone Suppression via Probability Mass Redistribution", **(SSC-L),** Sep 2019

87. **G. Nikandish, R. B. Staszewski, and A. Zhu,** "Broadband fully integrated GaN power amplifier with embedded minimum inductor bandpass filter and AM-PM compensation," **(SSC-L),** Sept. 2019

88. **K. Xu; F. Kuo; H. R. Chen; L. Cho; C. Jou; M. Chen; R. B. Staszewski,** "A 0.85mm2 51%-Efficient 11-dBm Compact DCO-DPA in 16-nm FinFET for Sub-Gigahertz IoT TX Using HD2 Self-Suppression and Pulling Mitigation", **(JSSC)** 2019

89. **J. Du, Y. Hu, T. Siriburanon, and R. B. Staszewski**, "A 0.3 V, 35% tuning-range, 60 kHz 1/f3-corner digitally controlled oscillator with vertically integrated switched capacitor banks achieving FoMT of -199 dB in 28-nm CMOS," **(CICC),** Apr. 2019

90. **V. Nguyen, F. Schembari, R. B. Staszewski,** "A 0.2-V 30-MS/s 11b-ENOB Open-Loop VCO-Based ADC in 28-nm CMOS", **SSC-L,** 2019

91. **M. P. Kennedy, Y. Donnelly, J. Breslin, S. Tulisi, S. Patil, C. Curtin, S. Brookes, B. Shelly, P. Griffin, M. Keaveney,** "4.48GHz 0.18µm SiGe BiCMOS Exact-Frequency Fractional-N Frequency Synthesizer with Spurious-Tone Suppression Yielding a -80dBc In-Band Fractional Spur", **(ISSCC),** Feb 2019

92. **N. Pourmousavian, F.W. Kuo, T. Siriburanon, M. Babaie, R. Staszewski.** "A 0.5-V 1.6-mW 2.4-GHz Fractional-N All-Digital PLL for Bluetooth LE with PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28-nm CMOS", IEEE Journal of Solid-State Circuits, Vol 53 Issue 9, Sep 2018 **(JSSC)**

93. **Y. Hu, T. Siriburanon, R. Staszewski.** "A Low-Flicker-Noise 30-GHz Class-F23 Oscillator in 28-nm CMOS Using Implicit Resonance and Explicit Common-Mode Return Path", IEEE Journal of Solid-State Circuits, July 2018 **(JSSC)**

94. **H. Wang, F. Schembari, M. Miśkowicz, R.B. Staszewski,** "An Adaptive-Resolution Quasi-Level-Crossing-Sampling ADC Based on Residue Quantization in 28-nm CMOS", IEEE Solid-State Circuits Letters **(SSC-L),** 2018

95. **Y. Li ; W. Cao ; A. Zhu,** "Instantaneous Sample Indexed Magnitude-Selective Affine Function-Based Behavioral Model for Digital Predistortion of RF Power Amplifiers", **(MTT),** 2018

96. **G. M. Salgado, A. Dicataldo, D. O'Hare, I. O'Connell, J. M. de la Rosa,** "Behavioural Modeling of SAR ADCs in Simulink", IEEE International Symposium on Circuits and Systems, **(ISCAS)** May 2018

97. **S. Asghar, S. Afridi, A. Pillai, A. Schuler, J. M. de la Rosa, I. O'Connell,** "A 2MS/S, 11.22 ENOB, 3.2 Vpp-D SAR ADC with Improved DNL and Offset Calculation", IEEE International Symposium on Circuits and Systems, **(ISCAS)** May 2018

98. **Y. Donnelly, H. Mo and M.P. Kennedy.** High-Speed Nested Cascaded MASH Digital Delta-Sigma Modulator-Based Divider Controller. In Proc. **ISCAS** 2018, May 2018.

99. A**. Salib; M. F. Flanagan; B. Cardiff,** "A Generic Foreground Calibration Algorithm for ADCs with Nonlinear Impairments", **(ISCAS),** May 2018

100. **W. Cao, Y. Li, and A. Zhu, (2017)** "Digital Suppression of Transmitter Leakage in FDD RF Transceivers: Aliasing Elimination and Model Selection," IEEE Transactions on Microwave Theory and Techniques, Vol. 65, early access, Dec. 2017 **(MTT)**

101. **Kelly, N. and Zhu, A. (2017)** 'Direct Error-Searching SPSA Based Model Extraction for Digital Predistortion of RF Power Amplifiers'. IEEE Transactions on Microwave Theory and Techniques, 65 **(MTT)**

102. **Wang, H., Li, G., Zhou, C., Tao, W., Liu, F., and Zhu, A. (2017)** '1-bit Observation for Direct-Learning-Based Digital Predistortion of RF Power Amplifiers'. IEEE Transactions on Microwave Theory and Techniques, 65 (07):2465-2475. **(MTT)**

103. **Cao, W., and Zhu, A. (2017)** 'A Modified Decomposed Vector Rotation-Based Behavioral Model With Efficient Hardware Implementation for Digital Predistortion of RF Power Amplifiers'. IEEE Transactions on Microwave Theory and Techniques, 65 (07):2443-2452 **(MTT)**

104. **Cao, W., Li, Y., and Zhu, A. (2017)** Magnitude-Selective Affine Function Based Digital Predistorter for RF Power Amplifiers in 5G Small-Cell Transmitters 2017 IEEE MTT-S International Microwave Symposium **(IMS)** Honolulu, Hawai'i, USA, June 2017

105. **Y. Hu, T. Siriburanon, R. Staszewski,** "A 30-GHz Class-F23 Oscillator in 28nm CMOS Using Harmonic Extraction and Achieving 120 kHz 1/f 3 Corner", **(ESSCIRC)** Sept 2017

106. **F. W. Kuo, N. Pourmousavian, T. Siriburanon, R. Staszewski,** "A 0.5V 1.6mW 2.4GHz Fractional-N All-Digital PLL for Bluetooth LE with PVT-Insensitive TDC using Switched-Capacitor Doubler in 28nm CMOS," IEEE **Symposium on VLSI Circuits,** June 2017

107. **A. Salib, B. Cardiff, M. F. Flanagan,** "A low-complexity correlation-based time skew estimation technique for time-interleaved SAR ADCs", Proc. of the IEEE International Symposium on Circuits and Systems **(ISCAS),** May 2017

108. **M.P. Kennedy, H. Mo and D. Mai.** "Nonlinearity-Induced Spurious Tones and Noise in Digitally-Assisted Frequency Synthesizers", In Proc. **ISCAS** 2017, pages ***-***, Baltimore, **-** May 2017.

109. **Xia, J., Yang, M., Guo, Y., and Zhu, A. (2016)** 'A Broadband High-Efficiency Doherty Power Amplifier with Integrated Compensating Reactance'. IEEE Transactions on Microwave Theory and Techniques, 64 (07):2014-2024. **(MTT)**

110. **Yang, M., Xia, J., Guo, Y., and Zhu, A. (2016)** 'Highly Efficient Broadband Continuous Inverse Class-F Power Amplifier Design Using Modified Elliptic Low-Pass Filtering Matching Network'. IEEE Transactions on Microwave Theory and Techniques, 64 (05):1515-1525. **(MTT)**

111. **Kelly, N., and Zhu, A. (2016)** 'Low Complexity Stochastic Optimization-Based Model Extraction for Digital Predistortion of RF Power Amplifiers'. IEEE Transactions on Microwave Theory and Techniques, 64 (05):1373-1382. **(MTT)**

112. **Yu, C., Sun, H., Zhu, X., Hong, W., and Zhu, A. (2016)** A Channelized Sideband Distortion Model for Suppressing Unwanted Emission of Q-band Millimeter Wave Transmitters 2016 IEEE MTT-S International Microwave Symposium **(IMS)** San Francisco, CA, USA, , 22-MAY-16 - 27-MAY-16

113. **M.P. Kennedy, H. Mo, Z. Huang and J.P. Lana.** A Method to Quantify the Dependence of Spur Heights on Offset Current in a CP-PLL. In Proc. **ISCAS,** May 2016.

114. **V. Marotta, G. Macera, M.P. Kennedy and E. Napoli**. Comparative Analysis of Differential Colpitts and Cross-Coupled VCOs in 180nm Si-Ge HBT. In Proc. **ISCAS,** May 2016.

115. **H. Mo, G. Hu and M.P. Kennedy.** Comparison of analytical predictions of the noise floor due to static charge pump mismatch in fractional-N frequency synthesizers. In Proc. **ISCAS,** May 2016.

116. **K. Sadeghipour et al,** "Design of a Sample-and-Hold Analog Front End for a 56Gb/s PAM-4 Receiver Using 65nm CMOS", International Symposium on Circuits and Systems **(ISCAS)** 2015

117. **Pepe D. et al,** "A 78.8-92.8 GHz 4-bit 0-360° Active Phase Shifter in 28nm FDSOI CMOS with 2.3 dB Average Peak Gain", Accepted for publication at IEEE European Solid State Circuits Conference **(ESSCIRC),** 2015

118. **Ossieur P., et al,** "A 1V 2mW 17GHz Multi-Modulus Frequency Divider Based on TSPC Logic Using 65nm CMOS", IEEE European Solid State Circuits Conference **(ESSCIRC),** 2014

119. **Kennedy M., et al.,** "0.3-4.3 GHz Frequency-Accurate Fractional-N Frequency Synthesizer with Integrated VCO and Nested Mixed-Radix Digital Delta-Sigma Modulator-Based Divider Controller", IEEE Journal of Solid State Circuits **(JSSC),** May 2014

120. N**.A. Quadir, et al,** "An inductorless linear optical receiver for 20Gbaud/s (40Gb/s) PAM-4 modulation using 28nm CMOS", International Symposium on CiLrcuits and Systems **(ISCAS),** Melbourne, Australia, June 2014

121. **Ossieur P., et al,** "A 10Gb/s Linear Burst-Mode Receiver in 0.25um SiGe:C BiCMOS", IEEE Journal of Solid State Circuits **(JSSC),** Feb 2013

122. **Kennedy M., et al.,** "High Speed, High Accuracy Fractional-N Frequency Synthesizer using Nested Mixed-Radix Digital Sigma-Delta Modulators", IEEE European Solid State Circuits Conference **(ESSCIRC),** Sep 2013

Highlight Publications

1. **V H Arzate-Palma, D G Rivera-Orozco, G M Salgado, F Sandoval-Ibarra,** "A Review on Fundamentals of Noise-Shaping SAR ADCs and Design Considerations," **Chips 2024,** May 2024
2. **B. O'Callaghan, D. R. Gawade, S. Kumar, D. O'Hare and J. L. Buckley,** "A Time-Efficient Model for Estimating Far-Field Wireless Power Transfer to Biomedical Implants," **2024 18th European Conference on Antennas and Propagation (EuCAP),** Mar 2024
3. **H. Shen, D. John and B. Cardiff,** "FEC-Aided Decision Feedback Blind Mismatch Calibration of TIADCs in Wireless Time-Varying Channel Environments," **in IEEE Transactions on Very Large Scale Integration (VLSI) Systems,** Jan 2024
4. **M. Saeed, O. Märtens, B. Larras, A. Frappé, D. John and B. Cardiff,** "ECG Classification With Event-Driven Sampling," **in IEEE Access, vol. 12, pp. 25188-25199, 2024,** Jan 2024
5. **Z. Zhang, D. Psychogious,** "Incorporating Directionality in Transversal-Resonator-Based Bandpass Filters With Tunable Transfer Function Characteristics", **TCAS-I,** Oct 2023
6. **X. Wang, M P Kennedy,** "Enhanced Jitter Analysis and Minimization for Digital PLLs With Mid-Rise TDCs and its Impact on Output Phase Noise", **TCAS-I,** Aug 2023
7. **B. O'Sullivan, Z. Pavlovic, N. Fiebig, C. O'Mathuna, S. O'Driscoll,** "Gate Driver Chip-Set using Low Volt-Second Pulse Transformer for Galvanic Signal Isolation", **APEC,** Mar 2023
8. **R. Beinarys, S. O'Driscoll, T.T. Vu,** "Flying Capacitor Voltage Imbalance Protection in Multilevel Bidirectional Inverters during Surge", **APEC,** Mar 2023
9. **A. John, A. Padinjarathala, E. Doheny, B. Cardiff, D. John,** "An evaluation of ECG data fusion algorithms for wearable IoT sensors", **J.InfFus,** Mar 2023
10. **G. Sivapalan, K. K. Nundy, A. James, B. Cardiff, D. John,** "Interpretable Rule Mining for Real-Time ECG Anomaly Detection in IoT Edge Sensors", **JIOT,** Mar 2023
11. **M.R.A. Naaser, D. Psychogiou,** "Acoustic Wave Resonator-Based Bandpass Filters With Continuously Tunable Fractional Bandwidth", **TCAS-II,** Dec 2022
12. **H. Shen, A. Blaq, D. John, B. Cardiff,** "A Foreground Mismatch and Memory Harmonic Distortion Calibration Algorithm for TIADC", **TCAS-I,** Dec 2022
13. **D. Mai, M P Kennedy,** "Optimized MASH-SR Divider Controller for Fractional-N Frequency Synthesizers", **TCAS-I,** Dec 2022
14. **V. Nguyen, F. Schembari, R. B. Staszewski,** "Exploring Speed Maximization of Frequency-to-Digital Conversion for Ultra-Low-Voltage VCO-Based ADCs", **TCAS-I,** Nov 2022
15. **E. Kobal, T. Siriburanon, R. B. Staszewski, A. Zhu,** "A Compact, Low-Power, Low-NF, Millimeter-Wave Cascode LNA With Magnetic Coupling Feedback in 22-nm FD-SOI CMOS for 5G Applications", **TCAS-II**, Nov 2022
16. **V. Mazzaro, M P Kennedy,** "A Family of Δ Modulators With High Spur Immunity and Low Folded Nonlinearity Noise When Used in Fractional- Frequency Synthesizers", **TCAS-I,** Aug 2022
17. **H. Shen, D. John, B. Cardiff,** "A Background Calibration for Joint Mismatch in the OFDM System With Time-Interleaved ADC", **TCAS-II,** June 2022
18. **E. Kobal, T. Siriburanon, X. Chen, H. M. Nguyen, R. B. Staszewski, A. Zhu,** "A Gm-Boosting Technique for Millimeter-Wave Low-Noise Amplifiers in 28-nm Triple-Well Bulk CMOS Using Floating Resistor in Body Biasing", **TCAS-I,** Aug 2022
19. **M.P. Kennedy, V. Mazzaro and D. Mai**, "Nonlinearity-Induced Spurs in Fractional-N Frequency Synthesizers", **TCAS-II,** Apr 2022
20. **Y. Hu, T. Siriburanon, R. B. Staszewski,** "Multirate Timestamp Modeling for Ultra-Low-Jitter Frequency Synthesis: A Tutorial", **TCAS-II,** Apr 2022
21. **H. M. Nguyen, F. Zhang, I. O'Connell, R. B. Staszewski, J. S. Walling,** "An Edge-Combining, Frequency Multiplying Class-D Power Amplifier", **TCAS-II,** Apr 2022

22. **Y. Kandeel, S. O'Driscoll, C. O'Mathuna, M. Duffy**, "Multiphase 3-Level Buck Passives Analysis Including 2- Phase Coupled Inductors", **APEC,** Mar 2022

23. **X. Chen, Y. Hu, T. Siriburanon, J. Du, R. B. Staszewski and A. Zhu,** "Flicker Phase-Noise Reduction Using Gate–Drain Phase Shift in Transformer-Based Oscillators", **TCAS-I,** Dec 2021

24. **Mazzaro V, Kennedy MP,** "Folded Noise Prediction in Nonlinear Fractional-N Frequency Synthesizers", **TCAS-I,** Aug 2021

25. **Avallone L, Mercandelli M, Santiccioli A, Kennedy MP, Levantino S, Samori C,** "A Comprehensive Phase Noise Analysis of Bang-Bang Digital PLLs", **TCAS-I,** Jul 2021

26. **Donnelly Y, Kennedy MP,** "An Algorithm for Implementing a Modulator Whose Output Is Spur-Free After Nonlinear Distortion", **TCAS-I,** July 2021

27. **A. Bozorg and R. B. Staszewski,** "A 20 MHz – 2 GHz Inductorless Two-Fold Noise-Canceling Low-Noise Amplifier in 28-nm CMOS," **TCAS-I,** July 2021

28. **G. R. Nikandish, A. Nasri, A. Yousefi, A. Zhu and R. B. Staszewski,** "A Broadband Fully Integrated Power Amplifier Using Waveform Shaping Multi-Resonance Harmonic Matching Network," **TCAS-I**, July 2021

29. **Mazzaro V, Kennedy MP,** "Spur Immunity in MASH-Based Fractional-N CP-PLLs with Polynomial Nonlinearities", **TCAS-I,** Jun 2021

30. **S. Hu, P. Chen, P. Quinlan and R. B. Staszewski,** "A 0.7-V Sub-mW Type-II Phase-Tracking Bluetooth Low Energy Receiver in 28-nm CMOS," **TCAS-I**, April. 2021

31. **R. Murphy, P. McCloskey, Z. Cao, C. Ó Mathúna, S. O'Driscoll,** "High Frequency Magnetic Sheet Materials – Performance Factor Comparisons and Design of Toroidal Inductors Embedded in PCB", **APEC,** June 2021

32. **A. John, S. J. Redmond, B. Cardiff, D. John,** "A Multimodal Data Fusion Technique for Heartbeat Detection in Wearable IoT Sensors", **JIOT,** June 2021

33. **F. Zhang, P. Chen, J. S. Walling, A. Zhu, R.B. Staszewski,** "An Active-under-Coil RFDAC with Analog Linear Interpolation in 28-nm CMOS", **TCAS-I,** Feb 2021

34. **Y. Hu, T. Siriburanon and R. B. Staszewski,** "Oscillator Flicker Phase Noise: A tutorial," **TCAS-II,** Feb. 2021

35. **A. Esmailiyan, J. Du, T. Siriburanon, F. Schembari and R. B. Staszewski,** "Dickson-charge-pump-based voltage-to-time conversion for time-based ADCs in 28nm CMOS," IEEE Open Journal of Circuits and Systems **(OJ-CAS),** Jan. 2021

36. **G. Nikandish, R. B. Staszewski and A. Zhu,** "A fully integrated GaN dual-channel power amplifier with crosstalk suppression for 5G massive MIMO transmitters," **TCAS-II,** Jan. 2021

37. **D. Mai, M. P. Kennedy,** "MASH-Based Divider Controllers for Mitigation of Wandering Spurs in a Fractional-N Frequency Synthesizer", **TCAS-I**, Jan 2021

38. **D. Mai, M. P. Kennedy,** "Influence of Initial Condition on Wandering Spur Pattern in a MASH-Based Fractional-N Frequency Synthesizer", **TCAS-II,** Dec 2020

39. **G.M. Salgado, D. O'Hare, I. O'Connell,** "Recent Advances and Trends in Noise Shaping SAR ADCs", **TCAS-II,** Dec 2020

40. **G. Nikandish, R. B. Staszewski and A. Zhu,** "Broadband Fully Integrated GaN Power Amplifier With Minimum-Inductance BPF Matching and Two-Transistor AM-PM Compensation," **TCAS-I,** Dec. 2020

41. **H. Wang, V. Nguyen, F. Schembari, and R. B. Staszewski**, "An adaptive-resolution quasi-level-crossing Delta modulator with VCO-based residue quantizer", **TCAS-II,** 2020

42. **J. Li, A. Ashraf, B. Cardiff, R. C. Panicker, Y. Lian and D. John,** "Low Power Optimisations for IoT Wearable Sensors Based on Evaluation of Nine QRS Detection Algorithms," in IEEE Open Journal of Circuits and Systems **(OJ-CAS),** Aug 2020

43. A**. Esmailiyan, F. Schembari, and R. B. Staszewski,** "A 0.36-V 5-MS/s time-mode flash ADC with Dickson-charge-pump-based comparators in 28-nm CMOS", **TCAS-I,** June 2020

44. **V. Mazzaro, M. P. Kennedy,** "Mitigation of "Horn Spurs" in a MASH-Based Fractional-N CP-PLL", **TCAS-II,** May 2020

45. **A. John, R. C. Panicker, B. Cardiff, Y. Lian and D. John,** "Binary Classifiers for Data Integrity Detection in Wearable IoT Edge Devices," in IEEE Open Journal of Circuits and Systems **(OJ-CAS),** April 2020

46. **D. Mai, M. P. Kennedy,** "Analysis of Wandering Spur Patterns in a Fractional-N Frequency Synthesizer with a MASH-Based Divider Controller", **TCAS-I,** Jan 2020

47. **L. Avallone, M. P. Kennedy, S. Karman, C. Samori, S. Levantino,** "Jitter Minimization in Digital PLLs with Mid-Rise TDCs", **TCAS-I,** Mar 2020

48. **A. Salib, B. Cardiff, M. F. Flanagan,** "Time-skew estimation for random sampling sequence time-interleaved ADCs", **TCAS-II,** Jan 2020

49. **H. Wang, F. Schembari, and R. B. Staszewski,** "Passive SC Δ modulator based on pipelined charge-sharing rotation in 28-nm CMOS," **TCAS-I,** Aug. 2019

50. **A. Salib; M. F. Flanagan; B. Cardiff,** "A Generic Foreground Calibration Algorithm for ADCs with Nonlinear Impairments", Vol 66, Issue 5, **TCAS-I,** May 2019

51. **A. Salib; M. F. Flanagan; B. Cardiff,** "A High-Precision Time Skew Estimation and Correction Technique for Time-Interleaved ADCs", **TCAS-I,** 2019

52. **Y. Donnelly; M. P. Kennedy** "Prediction of Phase Noise and Spurs in a Nonlinear Fractional-N Frequency Synthesizer" **TCAS-I,** July 2019

53. **V. O'Brien; B. Mullane,** "High Order Mismatch Shaping for Low Oversampling Rates", **TCAS-II,** March 2019

54. **Y. Donnelly, M. P. Kennedy,** "Wandering Spurs in MASH 1-1 Delta-Sigma Modulators", **TCAS-I**, Jul 2019

55. **Y. Hu, T. Siriburanon, and R. B. Staszewski,** "Intuitive understanding of flicker noise reduction via narrowing of conduction angle in voltage-biased oscillators", **TCAS-II,** 2019

56. **K-F. Un, F. Zhang, P-I. Mak, R. P. Martins, A. Zhu, R. Bogdan Staszewski.** "Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection", **TCAS-II,** March 2019

57. **Y. Hu; T. Siriburanon; R. B. Staszewski,** "Intuitive Understanding of Flicker Noise Reduction via Narrowing of Conduction Angle in Voltage-Biased Oscillators", **TCAS-II,** 2019

58. **P. Chen, X. Huang, Y. Chen, L. Wu, R. Staszewski.** "An On-Chip Self-Characterization of a Digital-to-Time Converter by Embedding it in a First-Order Δ Loop, **TCAS-I,** Aug 2018

59. **S. Asghar, S. Afridi, A. Pillai, A. Schuler, J. M. de la Rosa, I. O'Connell,** "A 2-MS/s, 11.22 ENOB, Extended Input Range SAR ADC With Improved DNL and Offset Calculation", **TCAS-I,** Nov 2018

60. **D. Mai and M.P. Kennedy.** "A Design Method for a Nested MASH-SQ Hybrid Divider Controller for Fractional-N Frequency Synthesizers", **TCAS-I,** April 2018.

61. **O'Connell, I, and O'Riordan, (2018)** "Techniques for reducing ULP device power consumption", Industry Session 5: Energy Harvesting, **APEC,** Mar 2018

62. **M. Keshavarz Hedayati; A. Abdipour; R. Sarraf Shirazi; C. Cetintepe; R. B. Staszewski,** "A 33-GHz LNA for 5G Wireless Systems in 28-nm Bulk CMOS", **TCAS-II,** Oct 2018

63. **D. Mai, H. Mo, M.P. Kennedy.** "Observations and Analysis of Wandering Spurs in MASH-Based Fractional-N Frequency Synthesizers". **TCAS-II,** May 2018.

64. **H. Mo and M.P. Kennedy.** "Masked Dithering of MASH Digital Delta-Sigma Modulators with Constant Inputs using Multiple Linear Feedback Shift Registers", **TCAS-I,** June 2017

65. **H. Mo and M.P. Kennedy.** "Influence of Initial Conditions on the Fundamental Periods of LFSR-Dithered MASH Digital Delta-Sigma Modulators with Constant Inputs", **TCAS-II,** Apr 2017.

66. **H. Mo and M.P. Kennedy.** "Masked Dithering of MASH Digital Delta-Sigma Modulators with Constant Inputs using Linear Feedback Shift Registers", **TCAS-I,** 2016

67. **Huang, G., Yu, C., and Zhu, A.,** "Analog Assisted Multichannel Digital Postcorrection for Time-Interleaved ADCs", **TCAS-II,** Feb 2016.

68. **H. Mo and M.P. Kennedy.** Influence of Initial Conditions on the Fundamental Periods of LFSR-Dithered MASH Digital Delta-Sigma Modulators with Constant Inputs. **TCAS-II,** 2016.

69. **Mooney J. et al,** "Dithered Multi-Bit Sigma-Delta Modulator Based DPWM for DC-DC Converters",

IEEE Applied Power Electronics Conference **APEC,** March 2015

70. **Halton M. et al,** "Robust Analysis and Synthesis Design Tools for Digitally Controlled Power Converters", IEEE Applied Power Electronics Conference **APEC,** March 2015

71. **Effler S., et al,** "Scalable Digital Power Controller with Phase Alignment and Frequency Synchronization", IEEE Transactions on Circuits and Systems I **(TCAS-I),** 2014

72. **Mooney J., et al,** "Application-Specific Instruction-Set Processor for Control of Multi-Rail DC-DC Converter Systems", IEEE Transactions on Circuits and Systems I **(TCAS-I),** Jan 2013

73. **Scharrer M., et al,** "Efficient Bi-directional Digital Communication Scheme for Isolated Switch Mode Power Converters", IEEE Transactions on Circuits and Systems I **(TCAS-I),** Dec 2012

MCCI
MICROELECTRONIC CIRCUITS CENTRE IRELAND

TECHNOLOGY CENTRE
ENTERPRISE IRELAND
IDA IRELAND SUPPORTED

Tyndall National Institute,
Dyke Parade,
Cork, Ireland,
T12 R5CP

+353 (0)21 2346056
info@mcci.ie
www.mcci.ie